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DESIGN OF A SHIP SERVICE CONVERTER MODULE FOR A REDUCED-SCALE PROTOTYPE INTEGRATED POWER SYSTEM

by

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DESIGN OF A SHIP SERVICE CONVERTER MODULE FOR A REDUCED-SCALE PROTOTYPE INTEGRATED POWER SYSTEM

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Submitted in partial fulfillment of the
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ABSTRACT

A DC Zonal Electrical Distribution System (DC ZEDS) is a strong candidate for the next generation surface combatant, DD-21. In order to equip DD-21 with DC ZEDS, preparative research includes the design of a low-power prototype Integrated Power System (IPS). This thesis examines the design and layout of one element of the IPS, a 500V/400V, 8kW, 20kHz dc-dc converter. The main thrust of the study is the documentation of product construction, design, and ancillary issues. Since the converter will be integrated into a testbed, it must be rugged, transportable, flexible, and provide convenient interconnection and monitoring. MATLAB and dSPACE models and circuit prototypes are implemented to validate subsystem designs and operation. Unit validation studies are conducted to assess performance of the power-section, controls, protection, and interfaces.

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EXECUTIVE SUMMARY

A 500V/400V, 8kW, 20kHz dc-dc converter has been developed in order to support ongoing research in Integrated Power Systems (IPS) and DC Zonal Electrical Distribution Systems (DC ZEDS). The Energy Sources Analysis Consortium (ESAC), consisting of researchers at the Naval Postgraduate School-Monterey, Purdue University, the University of Missouri at Rolla, the University of Wisconsin-Milwaukee, and the U.S. Naval Academy, have teamed to develop new technologies and use Commercial-Off-The Shelf (COTS) Technologies to support the development of prototype reduced-scale electric power distribution and propulsion systems for the next generation surface combatant, DD-21. The purpose of this thesis is to document the design and fabrication of one such prototype component: the Ship Service Converter Module (SSCM).

The SSCM consists of the following sub-sections/stages: input filter section, power section, IGBT driver board, main control stage (consisting of protection, start-up, buffering, Pulse-Width Modulation (PWM), and control circuitry), cooling and temperature control stage, power supply stage, and finally a user interface front panel. The main control stage contains a user select switch that provides the user with the following three options: (1) multi-loop control (the internal controller and PWM circuitry are utilized) where an external potentiometer allows the user to program the desired output voltage, (2) internal controller bypass (user inputs desired duty cycle and utilizes the internal PWM circuitry), and (3) internal controller and PWM circuitry bypass (user supplies external signal to gate the IGBT).

Design initiated with the selection of components for the SSCM that would meet or exceed the parameters specified by ESAC (P_{out} = 8kW, switching frequency = 20kHz, V_{in} = 500V/16A, R_{load} = 20Ω-200Ω, and V_{out} = 400V/20A at duty cycle 0.8). In addition to component selection, the electrical cabinet that houses the SSCM electronics was manufactured to be rugged, transportable, and provide accessible interconnections for both testing and monitoring. LED indicators were placed on the front panel to warn the user of an SSCM fault condition (i.e. over-current time out, 21.82A, and over

temperature, 70°C). Once the fault is cleared, reset pushbuttons on the front panel accommodate re-initiating operation.

The design equations for the dc-dc (buck) converter are well understood and were referenced to establish initial component design values. In order to ensure that the power section inductor maintains continuous current flow throughout the admissible load range, changes in permeability must be considered during design. For example, inductor permeability was found to change as much as 50% between full load (20Ω) and minimum load (200Ω). Applying the design equations, input filter and power section inductances are determined to be 0.4mH (0.357mH measured) and 1mH (0.99mH measured), respectively. Another example of component selection is circuit capacitance. Preliminary power section capacitance was determined by using the steady-state ripple constraint (12.5μF) and then was refined by using SIMULINK and MATLAB. Through simulation, it was determined that the circuit capacitance required to achieve a fast transient response (bandwidth of $\approx$500Hz), while not introducing duty cycle chattering, was 500μF. The input filter was designed to pass 360Hz and block 20kHz (switching frequency). The implemented filter achieved a 3dB frequency of 450Hz.

The dc-dc converter must provide stable and dependable voltage regulation. To achieve the aforementioned, a control circuit was designed. This project utilized a multi-loop closed-loop control, which makes use of the measured output voltage, output current, and inductor current to regulate the output voltage. Voltage (V_{out}) and current (i_L and i_{out}) sensing circuits were designed to provide input to the control circuitry. To verify stability (gain margin and phase margin), MATLAB code was written and Bode plots were generated. Further, the control circuit was placed on a breadboard and interfaced with dSPACE (hardware-in-the-loop) to prove stable operations were maintained throughout the entire load range. The duty cycle derived from the control circuitry is fed into the Pulse-Width Modulation (PWM) chip where the desired 20kHz switching frequency (20.4kHz measured) signal is produced to gate the IGBT.

This project also focused on the development of detailed schematic layouts and component part lists to assist in the fabrication of additional units at a later date by other ESAC contributors. PSPICE, SIMULINK, and Easytrax version 2.06 software packages were used to generate all schematics within this thesis. Component lead-time was a major factor during construction where parts can have up to a six-month delay time. Each sub-circuit (i.e. control, PWM, protection circuitry) is well documented and can be easily reproduced. Furthermore, the SSCM was designed with a user select switch thus providing the user with the option of internal or external control. The SSCM is designed to provide fault detection. Over-current time-out is provided should the inductor current increase beyond 21.82A while SSCM over-temperature is provided at 70°C. Front panel BNC connections are provided to monitor input and output current, input and output voltage, and duty cycle. Digital pictures were taken during the construction phase to further assist ESAC Universities in SSCM fabrication.

Detailed testing of the SSCM was performed in the lab and through simulation (SIMULINK and MATLAB). The SSCM was tested throughout the entire load range specified by ESAC and efficiency testing was performed on the unit. A detailed SIMULINK model was constructed to simulate the transient response of the dc-dc converter and control algorithm. Laboratory testing revealed that SSCM operation was in agreement with simulated results. The SSCM operated at 98.7% efficiency at full load and 96.1% at minimum load.

This research documented the design and construction of an 8kW dc-dc converter. The converter will be placed into a larger testbed for a small-scale Integrated Power System (IPS) to be assembled by ESAC. This SSCM will be transported to Missouri in order to support the fabrication of additional units. With IPS selected for DD-21, it is vital for research to continue in this area. Possible areas for future research include: soft switching units to increase efficiency, enhanced electrical shielding to prevent switching noise interference, fabrication of several SSCMs at various frequencies and power levels to compare efficiencies, and detailed use of dSPACE as a design tool. DC-DC converters

are an integral part of any DC distribution system and the Navy must continue with research in this area to ensure successful and reliable systems are delivered to the fleet.

I. INTRODUCTION

A. POWER DISTRIBUTION FOR NEXT GENERATION COMBATANT

In recent years with the collapse of the Soviet Union, Department of Defense expenditures have been scaled back. It has never been more important to develop systems that are cost effective, operationally flexible, and require fewer personnel. At the present, ac power distribution systems are the norm on U.S. Navy ships and many submarines; however, with the advent of new power electronic devices, research is focusing on dc power distribution. The U.S. Navy is actively investigating the implementation of a DC Zonal Electric Distribution System (DC ZEDS), versus a conventional ac radial or ac zonal distribution system, as a component of an Integrated Power System (IPS). AC zonal and DC zonal both have their advantages and disadvantages; however, it will be shown that survivability arguments strongly support dc distribution for the next generation warship.

Researchers at the U.S. Naval Postgraduate School-Monterey, Purdue University, the University of Missouri at Rolla, the University of Wisconsin-Milwaukee, and the U.S. Naval Academy have teamed to develop new technologies and use commercial-off-the shelf technologies (COTS) to support the development of prototype reduced-scale electric power distribution and propulsion systems for the next generation warship and submarine [1], [12]. The goal of this thesis is to document the design and fabrication of one such prototype component: the Ship Service Converter Module (SSCM).

B. ZONAL VERSUS RADIAL DISTRIBUTION

Many of today's naval combatants employ radial distribution. In this arrangement, typically three or four prime movers (gas turbine, steam turbine or diesel engine) drive generators that are connected to various switchboards co-located in the main machinery space. From the switchboards, 450V, 60Hz, three-phase ac is distributed to a number of load centers. The load centers in turn provide power to vital and nonvital

loads comprising ship service. Throughout the ship, transformers step 450V down to 115V for subsequent use at various ship service outlets. Obvious disadvantages of the radial distribution architecture include:

- suboptimal cable runs to supply alternate power to vital loads,
- weight addition from cable runs, switch gear, and transformers,
- a multitude of bulkhead penetrations implying that watertight integrity and survivability are jeopardized.

Zonal distribution employs a port and starboard main bus, and sections the ship into several electrical zones that are designed within watertight bulkheads. This design has the architectural advantage of accommodating cable installation in zones as the ship is constructed as illustrated in Figure (1-1) [2]. One of the main busses is located above the waterline, while the other main bus is below the waterline. This placement strategy maximizes the physical distance between busses and ensures maximum survivability during battle damage or collision [1].

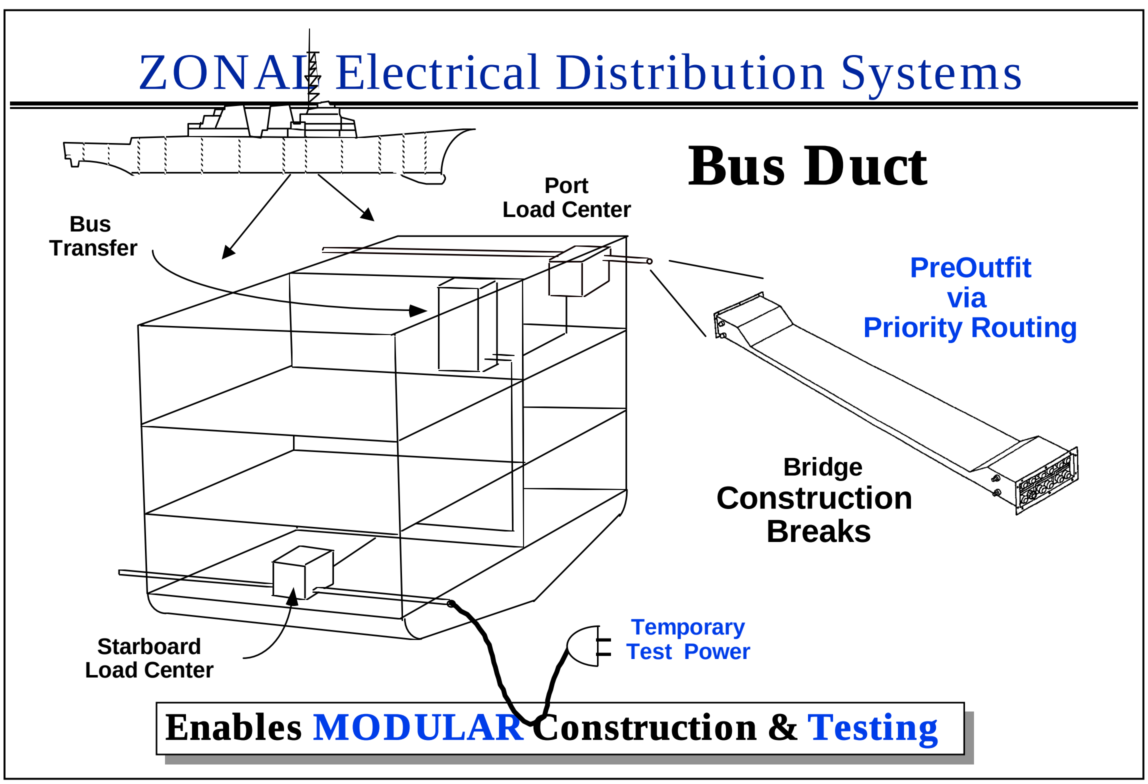

Figure 1-1, Modular Construction (From Ref. [2]).

In DC ZEDS, the port and starboard busses connect into a zone via load centers (dc-dc converters). The main bus dc voltage is stepped down within the zone and subsequently converted to three-phase ac or a lower level dc by additional converters within each zone. Vital loads, such as combat systems and navigation, are connected to both port and starboard load centers via an automatic bus transfer system (ABT). In one approach, if one bus were to fail, the remaining bus will supply continuous power to the load via an auctioneering process termed diode steering. Several advantages of ZEDS include:

- weight savings from reduced cabling as listed in Table (1-1) and Reference [1],
- no radically new converter architectures are required (though converter power density and reliability remain research issues),
- improved producibilty,
- reduced fire loading,
- only the main bus passes through watertight boundaries,
- modular ship fabrication,
- convenient installation and testing of electrical cable as zones are built.

Figure (1-2) illustrates the comparison between radial and zonal distribution [2] and Table (1-1) lists estimated weight savings [3,4]. With the removal of weight as indicated in Table (1-1), additional fuel, weapon, and cargo space will be available and further freedom in the design stage is achieved. Furthermore, in dc distribution, generator frequency is decoupled from the distribution requirements. This advantage will allow the prime mover/generator to be operated at its most efficient speed, resulting in fuel savings and lowering operational cost [4].

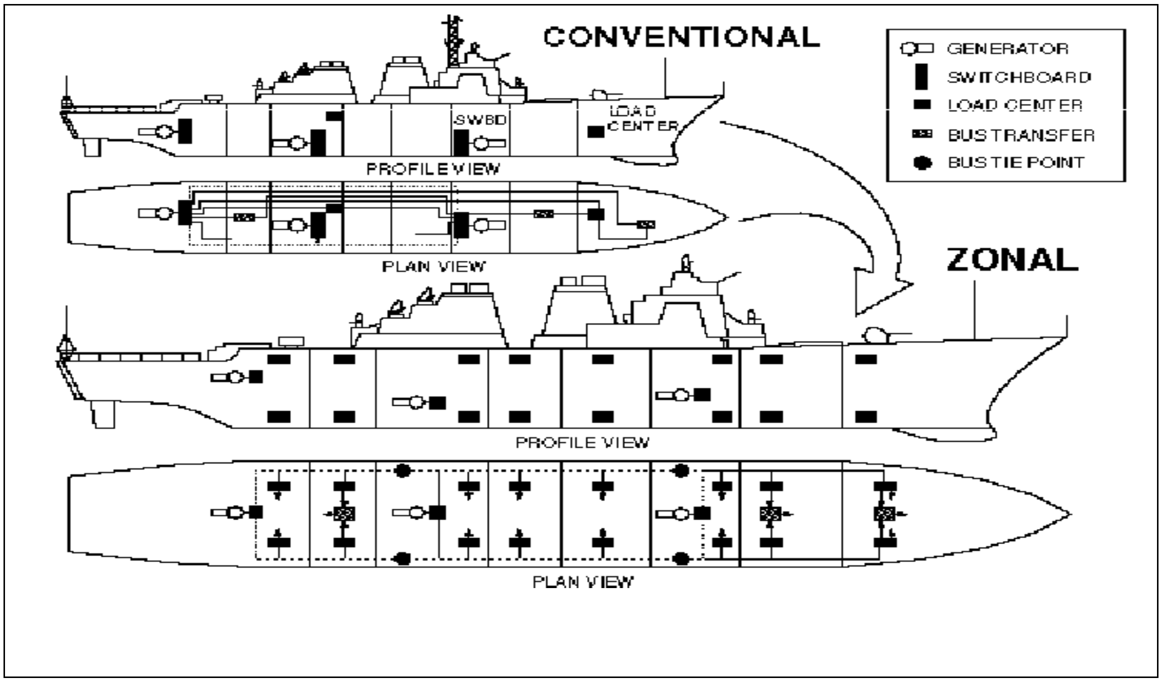

Figure 1-2, Radial vs. Zonal Distribution (From Ref. [2]).

Apparatus	Removal (LT)	Install (LT)	Net Change (LT)
Foundations	3.3	4.3	+1.0
Power Cables	116.7	79.8	-36.9
Switchgear	20.8	20.0	-0.8
Total	140.8	104.1	-36.7

Table 1-1. Zonal vs Conventional Architecture Weight Comparison (From Ref. [3]).

C. MAJOR COMPONENTS OF DC ZEDS

The major components involved in the DC ZEDS are outlined in Reference [1] and illustrated in Figure (1-3). Further component investigation is presented in later chapters.

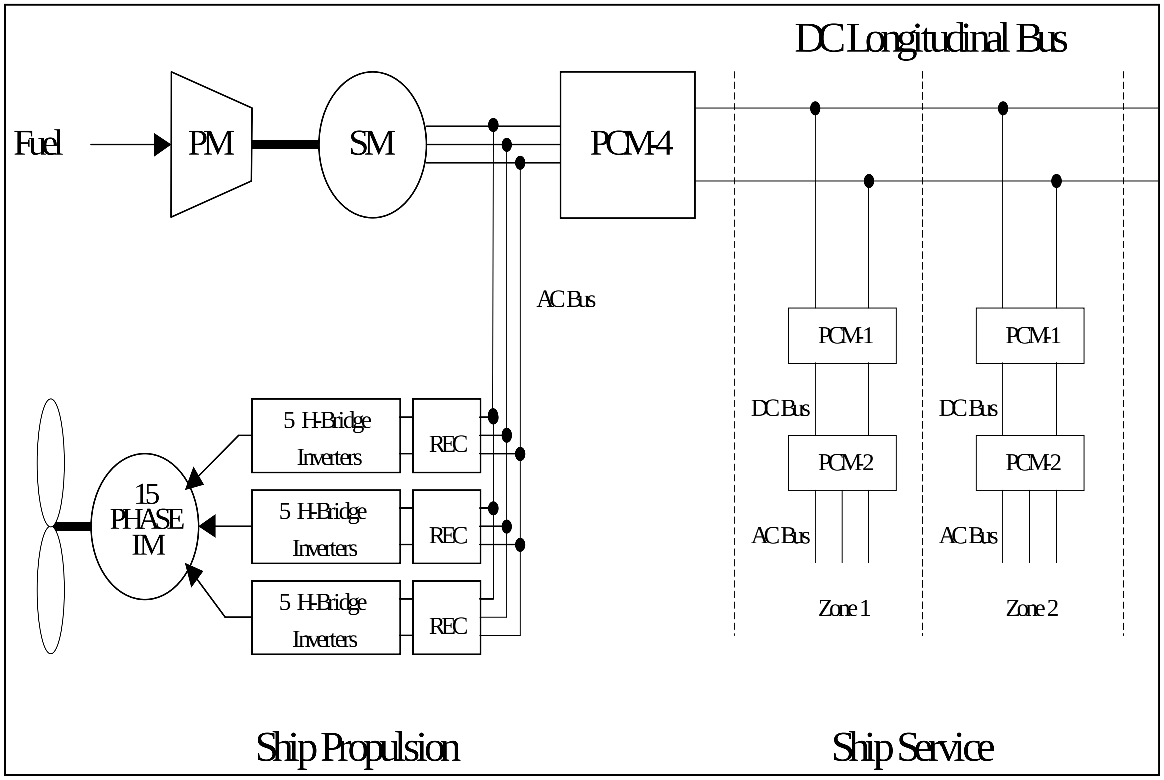

Figure 1-3, Portion of a Representative DC Zonal Architecture and IPS (From Ref. [2]).

From Figure (1-3), a prime mover powers an ac generator. The generator output is immediately rectified by Power Conversion Module four (PCM-4), one located on each bus, and routed to the port and starboard busses. Many options exist for this type of generator and several are listed in Reference [1].

From the port and starboard bus, high-voltage dc is routed through a Ship Service Converter Module (SSCM) labeled PCM-1 in Figure (1-3). Illustrated in Figure (1-4), is an SSCM in the form of a hard-switched dc-dc buck chopper that steps down the dc bus voltage and offers input buffering between the main bus and the loads within a zone. SSCMs must be capable of parallel operation, which will provide redundancy and satisfy anticipated zonal power requirements. PCM-1 may also supply additional dc-dc converters to achieve dc voltage levels appropriate for loads such as combat systems. The SSCM is the major component investigated in this thesis.

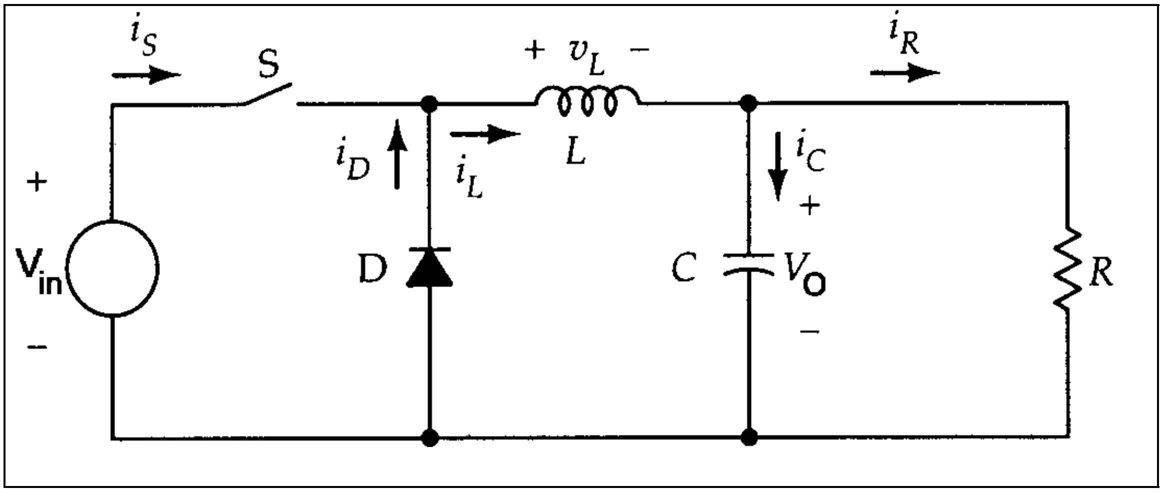

Figure 1-4, DC-DC Buck Chopper (From Ref. [1]).

The Ship Service Inverter Module (SSIM), labeled PCM-2 in Figure (1-3), supplies ac power. SSIMs convert the regulated output voltage from the SSCMs to low-distortion three-phase ac to drive different loads within a zone. SSIMs can be operated in parallel to offer redundancy and achieve power requirements within the zone.

The SSCMs and SSIMs are multi-functional components that implement current limiting, fault isolation, power conversion, regulation, and condition monitoring.

D. DC ZEDS RESEARCH CONDUCTED AT NPS

The Naval Postgraduate School has been actively involved in research for the next generation surface combatant. Several past theses have investigated issues relating to the DC Zonal Electrical Distribution System. The following is a short description of past theses. A more detailed list is contained in References [4] and [5].

- Constant power characteristics of DC ZEDS were investigated with reduced-order PSPICE dc-dc converter models. From these PSPICE models, observations were made concerning stability and controllability [6].
- ACSL models of a dc-dc converter and a three-phase inverter were developed. Closed-loop algorithms for buck choppers were investigated, and hardware-in-the-loop studies were conducted using a dSPACE card in order to validate computer models [7].

- The one-cycle control algorithm for a buck chopper was considered and implemented. Comparisons were made between the hardware and computer representation [8].
- Design and fabrication of several buck chopper power sections were documented [9].
- A voltage-mode buck controller was designed, along with the required gating circuitry. The associated analog hardware was built and documented [10].
- Frequency-based load sharing in current-mode controlled buck choppers was investigated and an ACSL model developed. In addition, an RMS frequency estimation circuit was designed and constructed in order to estimate the current from individual converters operating in parallel [11].

E. THESIS GOALS

The purpose of this thesis research is to thoroughly document the design and development of a Ship Service Converter Module (SSCM) for a reduced-scale prototype Integrated Power System (IPS). The Energy Sources Analysis Consortium (ESAC), consisting of Purdue University, the Naval Postgraduate School-Monterey, the U.S. Naval Academy, the University of Missouri-Rolla, and the University of Wisconsin-Milwaukee, have teamed to develop technologies which will support the electric power distribution and propulsion systems for the next generation of naval ships and submarines. Each institution has design responsibilities. Motivated by the proposal authored by personnel at Purdue University [12], the Naval Postgraduate School has designed, fabricated and validated a dc-dc converter using components described in Chapters II through IV. Easytrax, PSPICE, dSPACE, and MATLAB software were utilized throughout the design process. The reduced-scale SSCM will be inserted into a larger testbed as illustrated in Figure (1-5). The testbed is designed and configured to expedite the study of interconnection dynamics, stabilization algorithms, and input filter design. To achieve reliable performance in the testbed, the SSCM must be rugged, transportable, flexible, and provide convenient interconnection and monitoring capability.

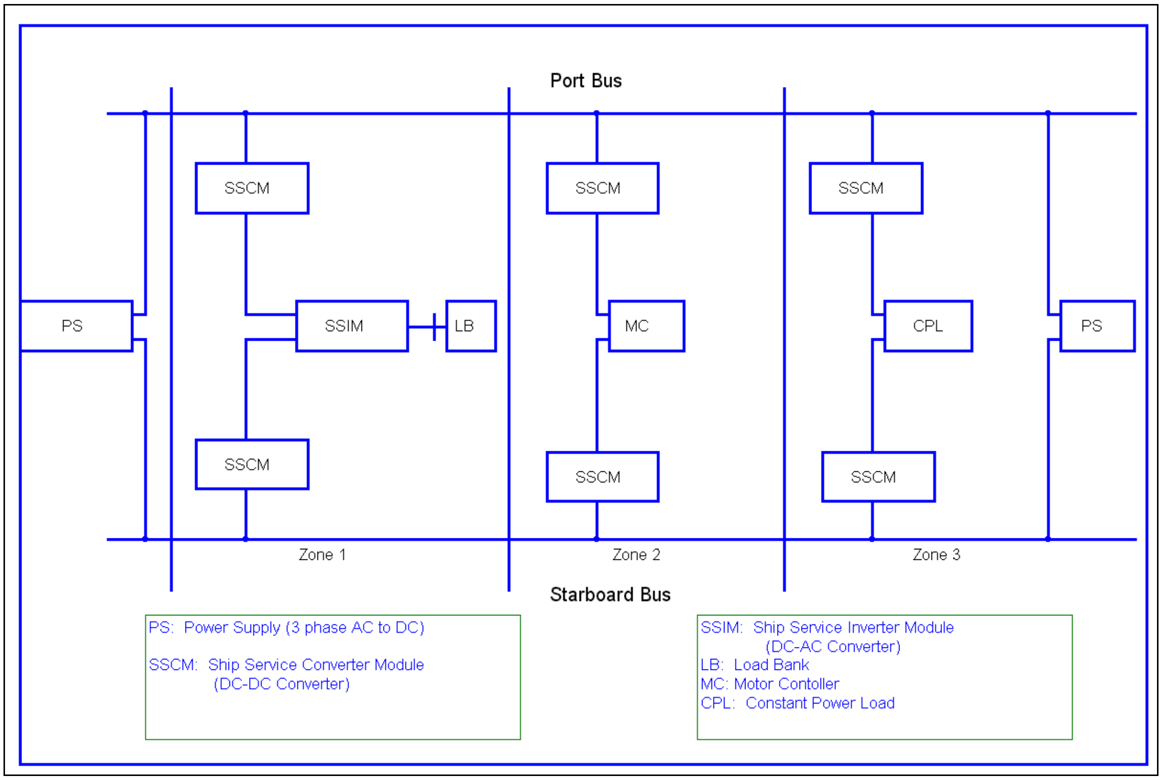

Figure 1-5, Proposed DC ZEDS Testbed (After Ref. [12]).

The work reported in this thesis provides detailed fabrication and design instructions to facilitate developing additional units and incorporating any required design modifications. This study directly supports ongoing research in the area of IPS for DD-21.

F. CHAPTER OVERVIEW

Chapter II covers the basic converter and testbed specifications. Chapter III focuses on the main component selection process for the dc-dc converter. Detailed steps for inductor design/selection are offered as well as guidelines for capacitor, Insulated Gate Bipolar Transistor (IGBT), and current sensor component selection. Chapter III concludes with a discussion of the pulse width modulation hardware. In Chapter IV, the control circuitry is investigated. Control board design from mathematical theory to hardware implementation is discussed. Additionally, the commercially-available IGBT driver board is explained and a test circuit is illustrated. Finally, Chapter IV contains a

description of the voltage and current sensing circuits. Chapter V documents and illustrates the overall SSCM layout where each section is broken down by circuit function (i.e. protection circuitry, PWM circuitry). Chapter VI includes a discussion of the testing and validation studies performed. Chapter VII contains concluding remarks and recommendations for future studies. Issues/recommendations are offered throughout the thesis where applicable.

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II. CONVERTER AND TESTBED SPECIFICATIONS

A. PURPOSE

As indicated in Chapter I, the goals of this thesis are to document the design, fabrication, and testing of a reduced-scale SSCM. The design must be rugged, flexible, transportable, and provide convenient connections for use in a larger testbed. This chapter will outline the specification requirements for the project, specify the general equations utilized in the design of a dc-dc converter, and provide an overview of the major assemblies required in this design.

B. SPECIFICATIONS

Table (2-1) lists the required specifications met in this design. Note, throughout this thesis the converter output voltage will be referred to as V_c or V_{out}, while the voltage applied to the input filter will be designated by V_{in} or E (see Figure (2-1)).

Parameter	**Buck Chopper**
Rated Continuous Output Power	8kW
Switching Frequency	20kHz
Input (maximum)	$V_{in} = E = 500V_{DC}$ $I_{in} = 16A$
Output (maximum)	$V_c = V_{out} = 400V_{DC}$ $I_{out} = 20A$
Range for Continuous Inductor Current	$\geq$10% Load ($R_L \leq 200\Omega$) at D $\geq$ 0.8
Output Voltage Ripple	$\leq$ 1% at Full Load

Table 2-1, Buck Converter Specifications.

1. Power Section

Figure (2-1) illustrates the basic elements of the selected power section for the dc-dc converter. From Reference [13], it can be shown that this dc-dc converter acts as a dc step-down (buck) transformer. The steady-state output voltage, V_c, is directly related to the nominal switch duty cycle (D) and, for an ideal converter, is given by Equation (2-1).

$$V_c = DE \tag{2-1}$$

To meet the input/output voltage specifications listed in Table (2-1), the nominal duty cycle must equal 0.8. Furthermore, components listed in Table (2-2) were selected with relevant data sheets contained in Appendix A. Analysis of each component is presented in detail in Chapter III.

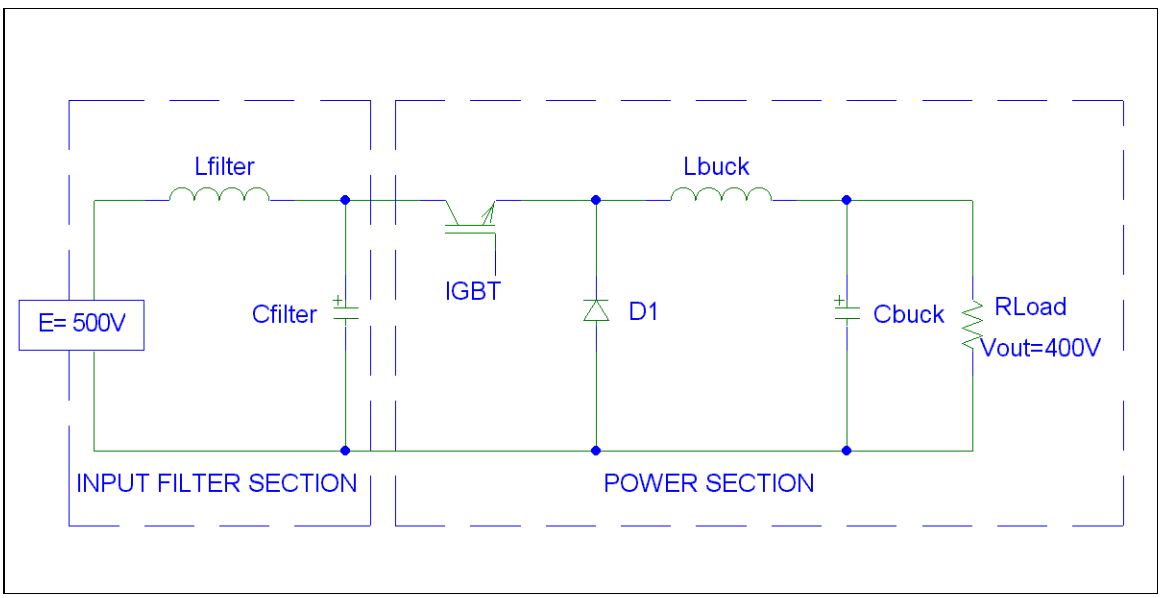


Figure 2-1, Buck Chopper Input Filter and Power Section.

Component	Manufacture/Part Number/Value
Input Filter Inductor	Arnold Cores (A-125112-2) 0.4 mH, hand wound, 55 turns, $\mu = 60$
Input Filter Capacitor Components	1) Mallory (CGH102T450V3L) 2-500 μF, 450V_{DC} 2) General Electric (Z97F8258) 1-45μF, 600V_{AC} 3) 3-2W, 3Ω resistors
Output Inductor	Arnold Cores (A-158304-2) 1.0 mH, hand wound, 57 turns, $\mu = 147$
Output Capacitor	Mallory (CGH102T450V3L) 500 μF, 450V_{DC}
Switch/Diode	Semikron (SKM-100GB-124D) IGBT Power Module, 1200V/100A

Table 2-2, Component Selection.

2. Input Filter

The input filter is illustrated in Figure (2-1). The assumed input to the filter is from a controlled six-pulse rectifier, which has a dc component of approximately 500V and the dominant ripple component at 360Hz. Pole placement for the two-pole filter was selected to allow 360Hz to pass while ensuring that 20kHz was blocked. The control should be able to accommodate the low-frequency ripple of the rectifier. Chapter III details the design process while Equation (2-2) provides the appropriate filter cutoff (3dB) frequency.

$$f_{filter} = \frac{1}{2\pi\sqrt{L_{filter}C_{filter}}} \tag{2-2}$$

3. Critical Inductance

Several factors are involved in the selection and design of the buck converter power section inductance (labeled L_{buck} in Figure (2-1)). Chapter III details the process involved in inductor design and Appendix B contains MATLAB code used to calculate inductance. Critical inductance is the minimum inductance required to maintain continuous conduction and is given by Equation (2-3). In Equation (2-3), T is the switching period (50μsec), R is the critical load resistance (R_{crit}=10R_{rated}), and D is the nominal duty cycle (0.8).

$$L_{crit} = \frac{TR}{2}(1-D) \qquad (2\text{-}3)$$

4. Capacitance

Capacitor selection was based on both voltage ripple and dynamic response. To meet the maximum one-percent steady-state ripple tolerance, Equation (2-4) from Reference [14] was utilized.

$$C_{min} = \frac{DT^2}{8\Delta V_c L}(V_{in} - V_{out}) \qquad (2\text{-}4)$$

In Equation (2-4), ΔV_c is the peak-to-peak capacitor voltage ripple, L is the actual power section inductance, and V_{in} and V_{out} are the nominal values. Chapter III details the minimum capacitance calculations and the actual findings and values utilized.

5. Switch/Diode

As stated previously, a Semikron IGBT was selected that met the switching speeds and the voltage and current ratings required for this design. Chapter III briefly

discusses the IGBT and Chapter IV details the design process and equations for the analog control board, IGBT driver board, and sensor boards. The power section diode, D1 in Figure (2-1), is physically contained inside the IGBT package. Since the diode is integrated in the same package, stray inductance in the circuit is minimized.

## C.	SSCM MONITORING AND INTERCONNECTIONS

Providing the ability to monitor key circuit parameters in any system is vital to the user. As illustrated in Figure (2-2), the front panel of the SSCM was designed to provide continuous system monitoring and testing capability. All British Naval Connector (BNC)

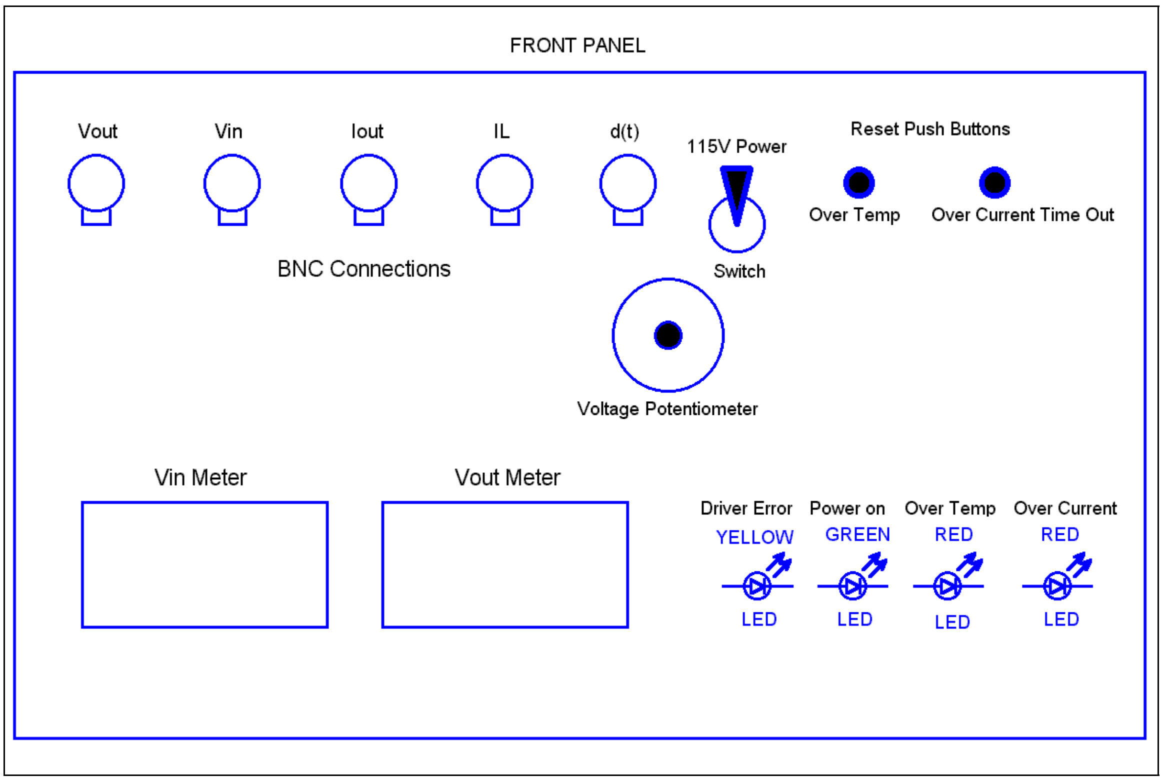


Figure 2-2, SSCM Front Panel.

connections are accessible and easily replaced. The BNC connections displayed in Figure (2-2) are connected via cables to easily accessible BNC connections located on top of the main SSCM circuit board. Digital meters were provided to give precise readouts of input and output voltage. Light Emitting Diodes (LEDs) are mounted on the

front panel to warn the user of a fault and to display SSCM power status. Fault LEDs and associated protection circuitry are discussed in Chapter V.

To provide control option flexibility, the SSCM contains a user select switch (SW1) located on the main circuit board. The switch is illustrated in Figure (2-3) along with a description of switch functional positions. To interpret the table in Figure (2-3), the following is offered. If the user desires to use the SSCM internal control and PWM circuitry, SW1 toggles 1 and 2 are placed in the "on" position while 3 and 4 are down or "off" (the down position has no label). If the user desires to provide an external duty cycle to the PWM circuit and bypass the internal control circuitry, then the desired duty cycle is input into the front panel BNC at d(t) and SW1 toggles 2 and 3 are placed "on" while SW1 toggles 1 and 4 are "off". Finally, if only an external duty cycle is desired (by pass both the internal controller and PWM circuit), SW1 toggle 4 is set in the "on" position and all other remaining toggles are "off." The SSCM was shipped in the test mode, which indicates that the SSCM is utilizing the internal integral controller and PWM circuit (1 and 2 "on"). Figure (2-3) is for illustrative purposes only, switch interface and a detailed schematic are offered in Chapter V.

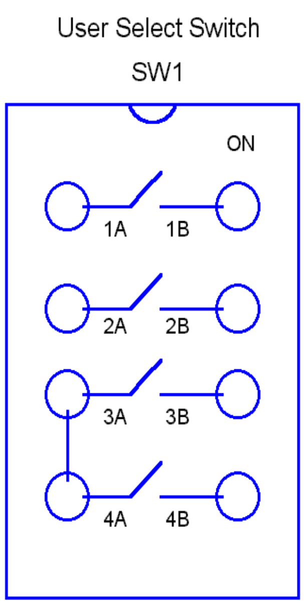


Table for switch (SW1)

SW1-	POSITION	FUNCTION
4	ON	Connects Front Panel directly to IGBT Driver 0-15V
3	ON	Connects Front Panel to PWM input 0-10V d(t)
2	ON	NOTE: Close together, uses external duty cycle signal
2	ON	Test Mode Integral Contoller
1	ON	NOTE: Close together, uses SSCM controller and PWM chip

Figure 2-3, User Select Switch.

D. SYSTEM COOLING AND PROTECTION

1. System Cooling

SSCM cooling was achieved by the use of two 115Vac/60Hz (4-5/8") Globe Motors fans (part# A47-B15A-15T3-000). One fan was mounted directly onto the rear panel and forced air into the SSCM at approximately 100 CFM while the second fan was mounted directly to the heat sink to force the air across the fins of the heat sink and back out the rear panel of the SSCM. Figure (2-4) illustrates fan placement on the rear panel while Figure (2-5) illustrates the rear and side view of the IGBT placement. Placing the IGBT on the side of the heat sink allowed heat generated from the IGBT to transfer down the fins of the heat sink. These fins are in the path of the fan thus allowing heat to be immediately removed from the enclosure.

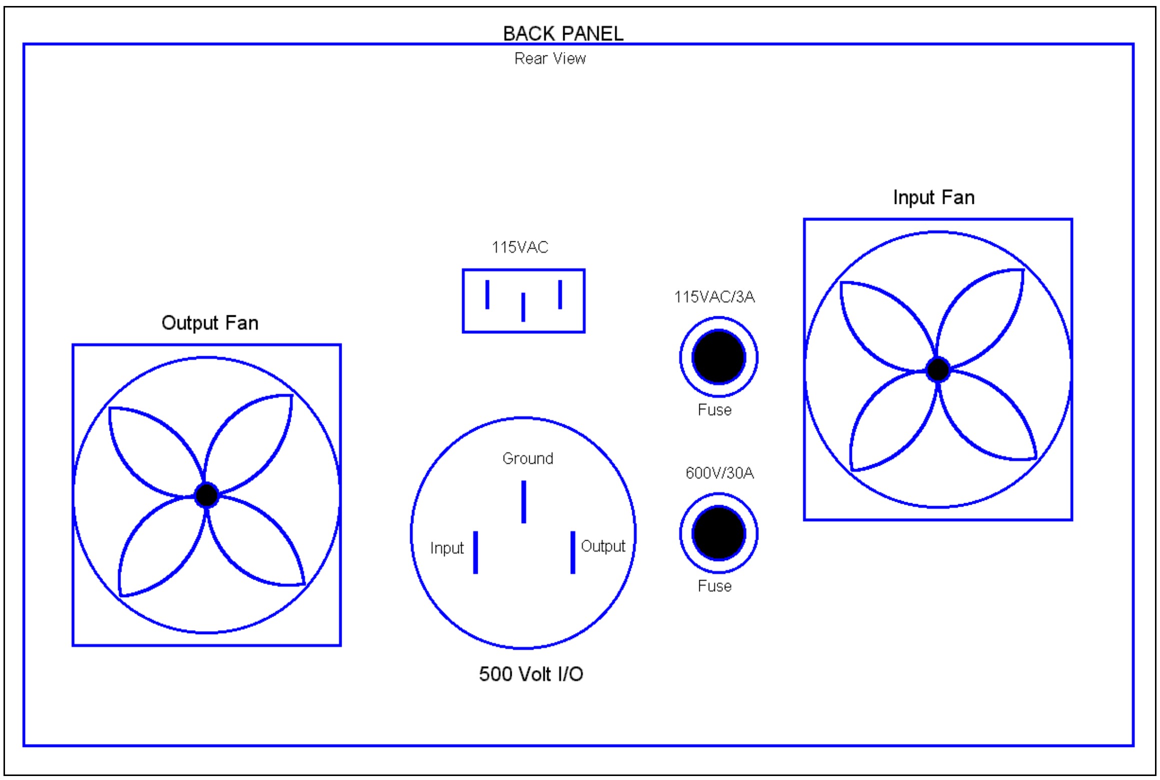


Figure 2-4, SSCM Back Panel.

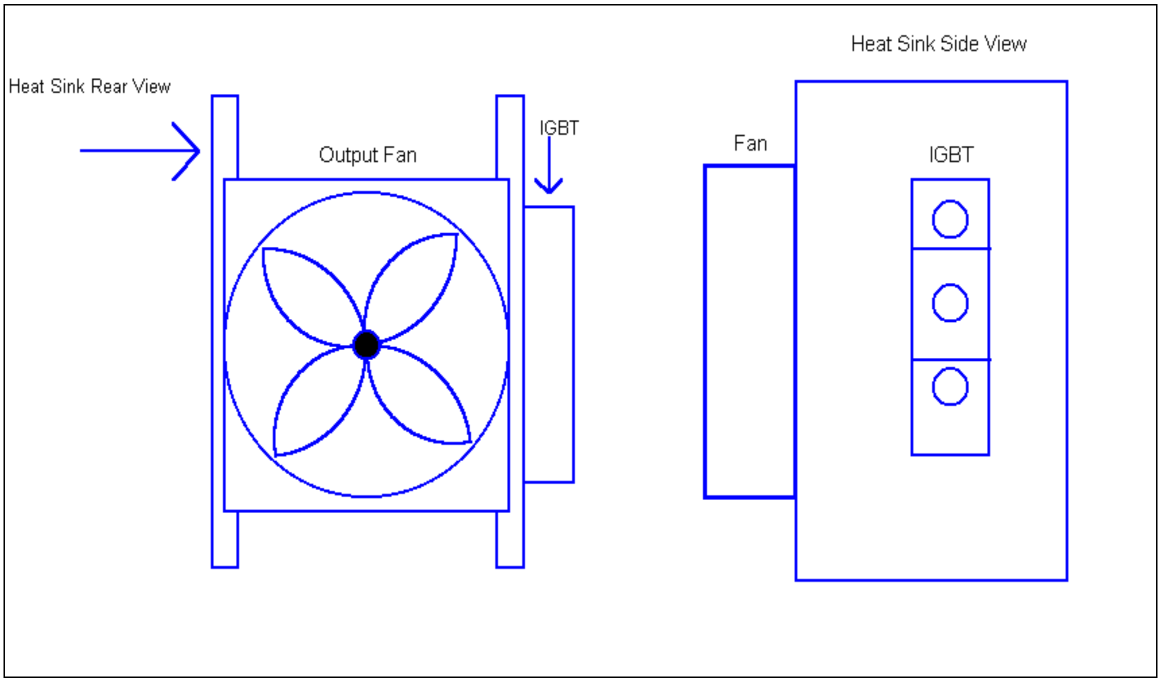


Figure 2-5, Heat Sink Layout.

2. Protection Circuitry

The protection circuit is discussed in detail in Chapter V. From Figure (2-2), the SSCM provides indication of over-current and over-temperature by the use of two red LEDs. Reset buttons are located on the front panel should the aforementioned faults occur. Currently, "driver board error", caused either by an IGBT short circuit or a supply under-voltage condition ($<\approx$11V), is indicated by converter lockout (driver board no longer gates the IGBT). If this happens, all power must be removed from the converter and control power cycled off-on to reset the driver board. A yellow LED (not connected) was placed in the front panel (see Figure (2-2)) if future hardware monitoring of the "driver board error" is desired. Currently, there is no LED indication for "driver board error."

E. DC ZEDS TESTBED

As outlined in Reference [12], the objective of ESAC will be to construct a laboratory-scale DC ZEDS distribution system. It is anticipated that a three-zone system will be constructed. The rating for the entire system will be on the order of 15kW. This system will be used to

- Provide a testbed for research in control and automation tools developed by ESAC,
- Provide a testbed for research in CAD Tools developed by ESAC,
- Serve as a baseline for comparison to the full-scale advanced development system,
- Serve as a basis for future support of the LBES (Land Base Engineering Site) test site (it would allow experiments and studies, which do not risk hardware, to be performed at lower power levels prior to testing at LBES) or to demonstrate new controls concepts before retrofits to LBES,
- Serve as a resource to the academic and industrial community in general by providing a thoroughly documented system on which to demonstrate controls and CAD tools developed by other researchers.

As stated in Reference [12], the system will be carefully documented and the documentation will be placed on the web so that it will also be a resource to researchers not directly involved in this project. Deliverables will include the hardware demonstration and a web-based report with studies, which will be made available to the entire engineering community. The schedule for this task is as follows: months 1-8 encompass component construction, months 9-15 entail system integration and studies, months 16-18 are reserved for reporting. The periods mentioned begin January 2001.

As stated in Chapter I, NPS is responsible for the SSCM. The bulleted list above pertains to the entire ESAC. The chapters and appendices that follow comprehensively document the SSCM design process.

F. SUMMARY

This chapter provided an overview of the general design equations, physical cabinet appearance, and a brief discussion of system cooling and protection. Furthermore, the ESAC outline for all schools involved was restated from Reference [12]. Chapter III details the component selection process for the SSCM designed at NPS.

III. COMPONENT SELECTION

A. PURPOSE

The purpose of this chapter is to document the design process and component selection for the buck converter (SSCM).

B. COMPONENT SELECTION

Basic converter specifications, Table (2-1), were developed based on ESAC's project needs, component cost, and practicality of fabrication. The following subsections provide the design details for the main inductor, output capacitor, input filter, current sensors, pulse-width-modulation circuitry, and IGBT.

1. Power Section Inductor Design

Design for the buck chopper inductor was carried out in accordance with Reference [14]. Table (3-1) defines the terms utilized in inductor design.

Parameter	Definition	Units of Measure
B_{max}	Maximum Flux Density	Gauss
E_{rms}	Equivalent Sinusoidal rms Voltage	Volts
A_e	Effective Cross Sectional Area of Magnetic Path	cm^2
N	Number of Turns	Dimensionless
F	Frequency	Hertz
H	Magnetizing Force	Oersteds
I	Peak Current	Amperes
l_e	Effective Magnetic Path Length	cm
L_{1000}	Inductance Factor	milli-Henries
μ	Permeability	Henries/inch
B	Flux Density	Gauss
Ht	Core Height	Inches
H_e	Effective Height Before Finish	Inches
L	Measured Inductance	Henries
Q	Quality Factor	Dimensionless
ω	Radian Frequency $2\pi f$	Rad/sec

Table 3-1, Inductor Component Design.

The buck chopper inductor was sized to maintain continuous inductor current over a load range of 10% to 100% rated. The most limiting condition for continuous inductor current occurs at minimum load. To maintain continuous operation, the inductor must be wound to meet or exceed the critical inductance for the circuit. Reference [15] defines critical inductance, with the result given by Equation (3-1) where T is the switching period, R is the resistance at minimum load, and D is the nominal switch duty cycle.

$$L_{crit} = \frac{TR}{2}(1-D) \tag{3-1}$$

By design, the switching frequency was chosen to be 20kHz or T=50μsec. As outlined in Reference [10], this selection of switching frequency provides the following advantages:

- achieves the maximum switching frequency for hard-switched IGBTs at these power levels,
- eliminates audible switching noise of the buck chopper,
- minimizes the required inductor size,
- minimizes the inductor ripple current given by $\Delta I = \frac{E - V_c}{L}(DT)$,
- maximizes the allowable closed-loop control bandwidth.

Analyzing Equation (3-1), two of the input parameters are set, T and R. D is determined using Equation (3-2) and is given by

$$D = \frac{V_c}{E} = \frac{400V}{500V} = 0.8 \tag{3-2}$$

Load resistance ranges from 20Ω (100%) to 200Ω (10%). For R=200Ω, L_{crit}=1mH. An inductance of 1mH was selected to satisfy the continuous current requirement while minimizing the inductor size.

Following a full development in Reference [14], core sizes for the input filter (to be discussed in a later section) and buck chopper were determined to be 60μ and 147μ, respectively, as listed in Table (2-2). The following discussion details the design process utilized for the power section inductor (similar steps apply for the input filter inductor design).

As indicated in Table (2-1), up to an average of 20A of current will flow through the main inductor. With this in mind, Table (3-2) was referenced to determine that 12-gauge wire would meet the current specification.

AWG	Feet/Ohm	Ohms/100ft	Ampacity	mm^2	Meters/Ohm	Ohms/100M
10	490.2	.204	30	2.588	149.5	.669
12	308.7	.324	20	2.053	94.1	1.06
14	193.8	.516	15	1.628	59.1	1.69
16	122.3	.818	10	1.291	37.3	2.68
18	76.8	1.30	5	1.024	23.4	4.27

Table 3-2, Copper Wire Resistance Table (After Ref. [16]).

Next, based on the fact that the inductance was determined to be 1mH and I = 20A, the calculation of the product LI^2 (energy) yields 0.4 Joules. Figure (3-1) from Reference [17] was consulted to determine a required core weight. Entering Figure (3-1) horizontally at LI^2 = 0.4, the line is intersected at a required core weight of approximately ($\approx$) 2.6 lbs. Returning to Reference [14], the 5.218-inch core met specifications.

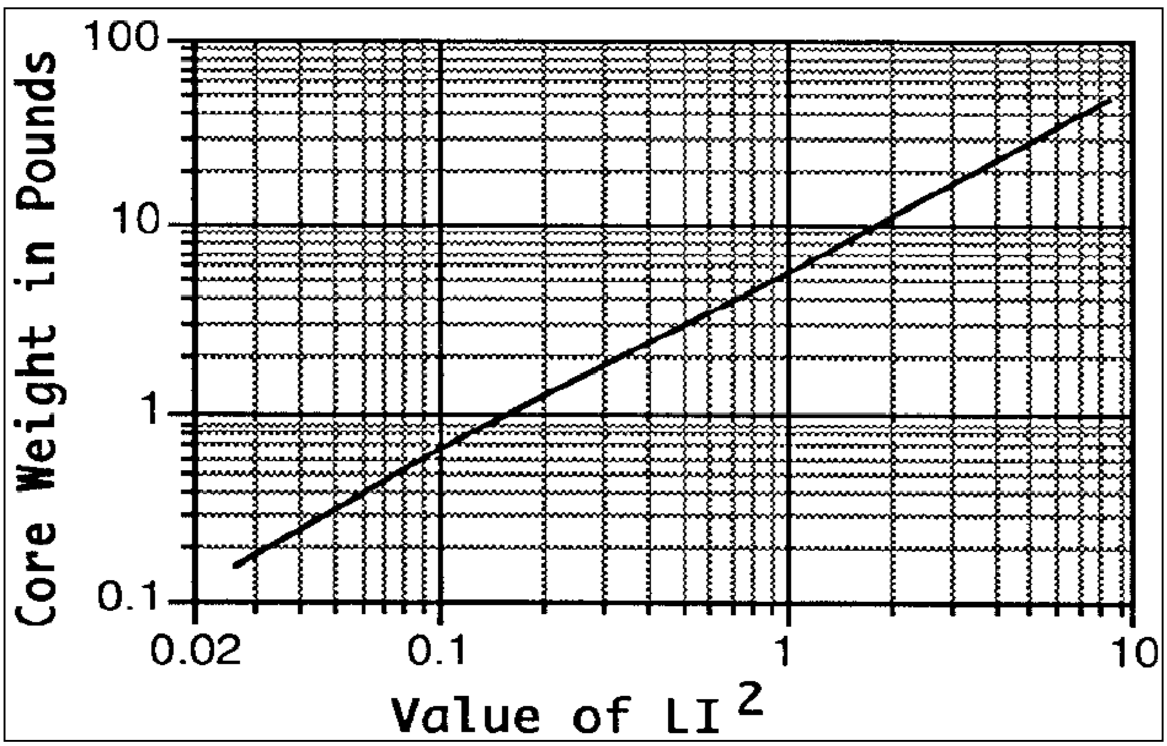


Figure 3-1, Core Weight (From Ref. [17]).

The number of turns for the inductor (N) was calculated using Equation (3-3) and Reference [14].

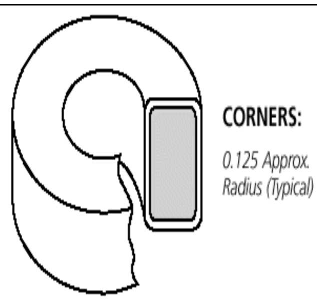
$$N = 1000\sqrt{\frac{L}{L_{1000}}} \tag{3-3}$$

With L = 1mH and L_{1000} = 304mH, listed in Reference [14], N was approximately equal to 57 turns.

The magnetizing force (H) was then computed using Equation (3-4).

$$H = \frac{0.4\pi NI}{l_e} \tag{3-4}$$

Employing the effective magnetic path dimension (33.12cm) listed in Figure (3-2), H was calculated to be 43.25 Oersteds. Note, Figure (3-2) is for a 125μ inductor; however, the information illustrated here is the same as that for the 147μ inductor.



Dimensions

	Outside Diameter	Inside Diameter	Height
Before Coating Nominal	5.218 in 132.54 mm	3.094 in 78.59 mm	0.800 in 20.32 mm
After Coating (Blue Epoxy)	5.274 in Max. 133.96 mm Max.	3.033 in Min. 77.04 mm Min.	0.855 in Max. 21.72 mm Max.

Physical Specifications

Effective Cross Sectional Area of Magnetic Path, A_e (Reference)	Effective Magnetic Path Length, l_e (Reference)	Effective Core Volume, V_e (Reference)	Minimum Window Area (Reference)	Approximate Weight of Finished 125μ MPP Core	Approximate Mean Length of Turn for Full Winding (Half of I.D. Remaining)
0.8288 in^2 5.3471 cm^2	12.767 in 33.12 cm	10.58 in^3 173.40 cm^3	7.225 in^2 46.612 cm^2 9,199,089 cmil	3.19 lbs 1450 g	3.97 in 10.09 cm

Figure 3-2, Core Dimensions 5.218 Inch (From Ref. [14]).

Continuing, B_{max} was determined using Equation (3-5) from Reference [14] where N = 57, A_e = 5.3471cm^2, f = 20kHz.

$$B_{max} = \frac{E_{rms} \times 10^8}{\sqrt{2}\pi N A_e f} \tag{3-5}$$

Equation (3-5) is valid for sinusoidal voltages. With a nominal duty cycle of 0.8 and 500V input voltage, the steady-state ideal inductor voltage is as given in Figure (3-3) plot (A): at 100V for 80% of the switching period, at -400V for 20% of the switching period.

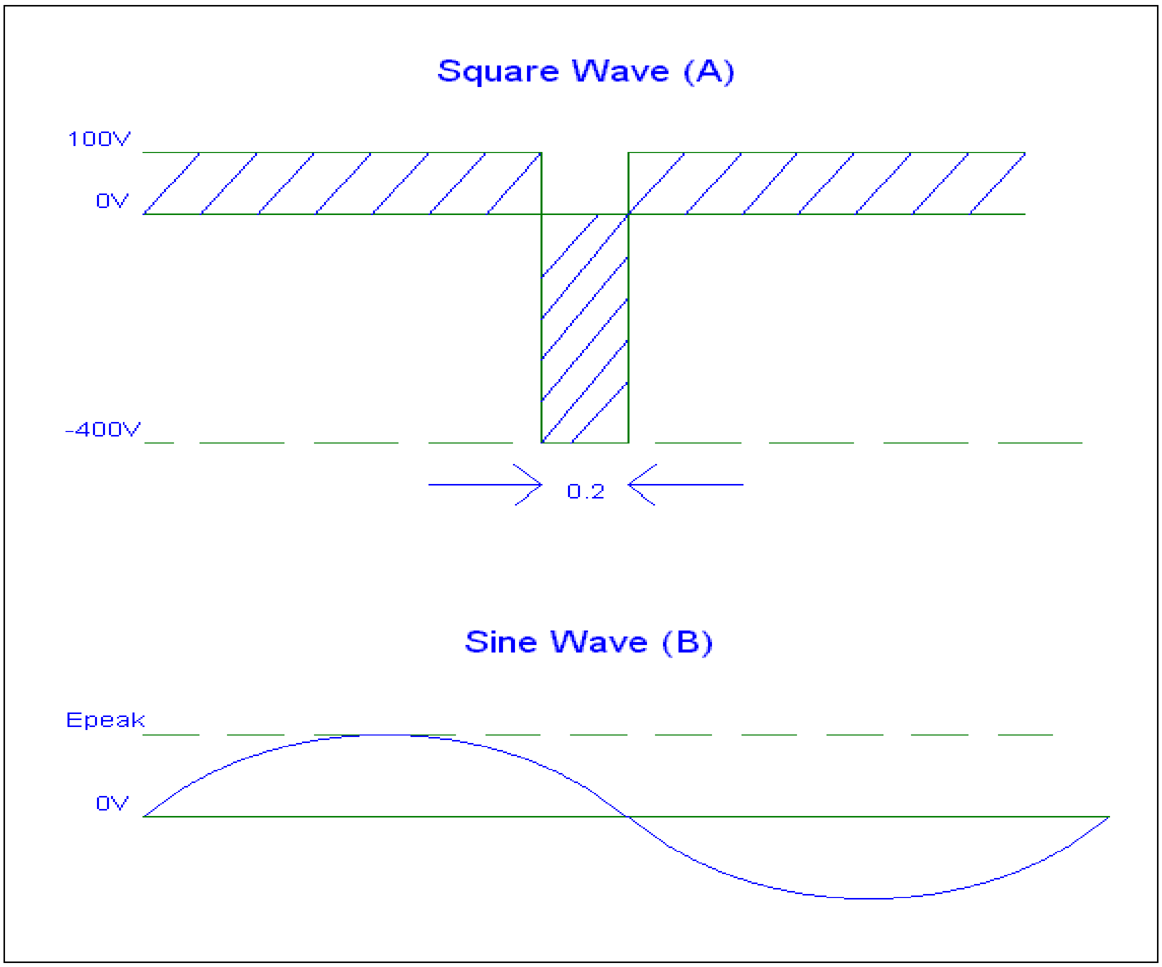


Figure 3-3, Illustrations of Waveforms for Equations (3-5) and (3-7).

From Figure (3-3) plot (A), the area above the 0V-Reference line must be equal to the area below the 0V-Reference. This is a necessary condition for the circuit to be in the steady state. With this in mind, the following must be true: E_{p+} D = E_{p-}(1-D) where E_{p+} is the positive peak (+100V) and E_{p-} is the negative peak (-400V). The same can be said about plot (B) of Figure (3-3): the area above 0V must equal the area below 0V. As a result, Equation (3-6) can be derived.

$$\frac{\sqrt{2}E_{rms}}{\pi} = E_{peak}D \qquad (3\text{-}6)$$

The left hand side of Equation (3-6) applies to plot (B) while the right hand side of Equation (3-6) applies to plot (A). The first term on the left hand side of Equation (3-6) is the area of one-half cycle of a sine wave and the first term on the right hand side is the area of a rectangle, the units are in agreement and Equation (3-6) is valid. Therefore, based on the anticipated quasi-rectangular voltage waveform, Equation (3-5) will take the form of Equation (3-7).

$$B_{max} = \frac{E_{peak} \times 10^{8} \times D}{2NA_{e}f} \qquad (3\text{-}7)$$

In Equation (3-7), f is the switching frequency in Hz and D is the nominal duty cycle. Substituting all values into Equation (3-7) with D = 0.8 and E_{peak} = 100V yields B_{max} = 657.07 Gauss. It should be noted that the same result can be reached by setting D = 0.2 and E_{peak} = 400V

Permeability (μ), for the core was determined using Equation (3-8) where (l_e) and (A_e) were defined in Table (3-1) and given in Reference [14] and L is in nano-henries ($1\text{x}10^6$nH).

$$\mu = \frac{Ll_e}{4\pi A_e N^2} \tag{3-8}$$

Substituting all values into Equation (3-8), a permeability of approximately 152 was determined. The closest μ commercially available from Arnold Cores was 147μ; therefore, this core was utilized for this project.

Finally, consulting Figure (3-4) with the horizontal argument of 43.25 Oersteds (from Equation (3-4)), the 147μ line is intersected at approximately 4700 gauss. From the graph, the inductor remains within the linear range of 4700 gauss plus or minus 657.07 gauss (determined from Equation (3-7)). As determined from the graph in Figure (3-4), it is evident that the 147μ curve remains in the linear region and saturation does not occur. The inductors were wound in the lab and measured using available lab equipment (Sencore model LC53 "Z meter" capacitor-inductor Analyzer). The 147μ/57turn/1mH inductor possessed a measured inductance of 0.99mH (at zero current).

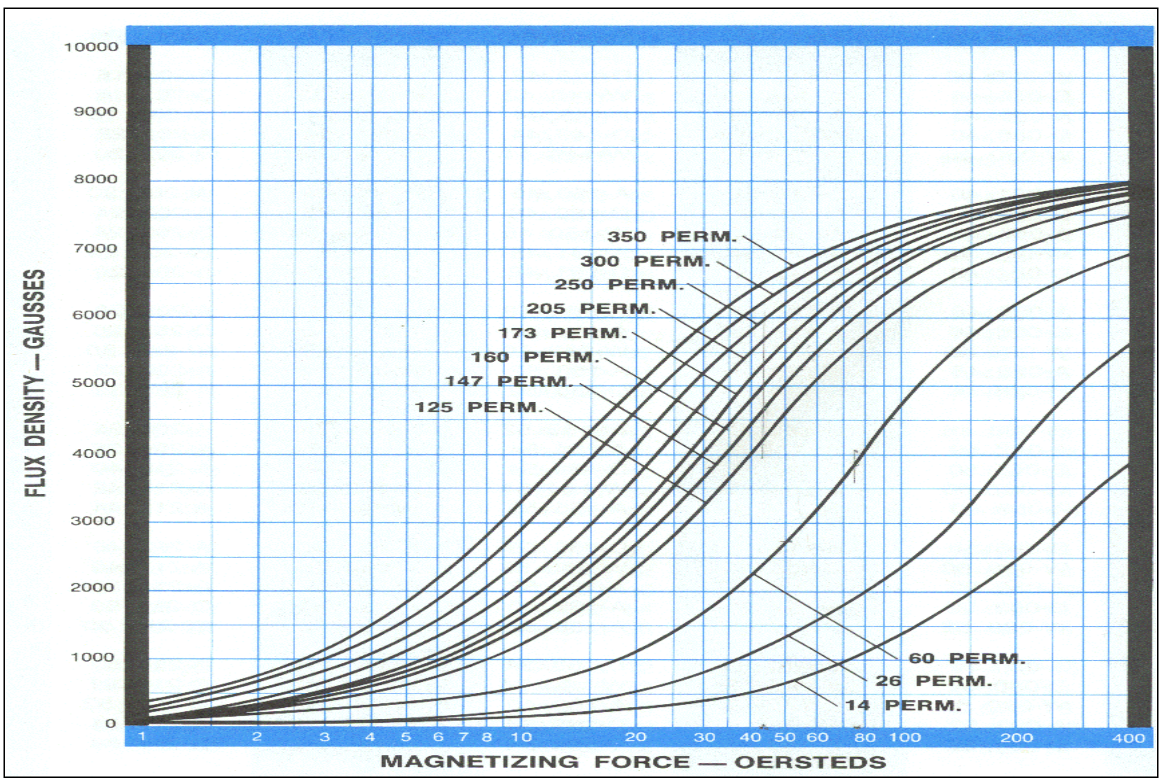


Figure 3-4, B-H Curves (From Ref. [14]).

Reference [14] utilizes the CGS system. If it is desired to use the SI system, Table (3-3) from Reference [14] can be entered to convert between the two systems.

Quantity	**To Convert**		**Multiply By**
	From	**To**	
Magnetic Flux Density (B)	Gauss (CGS)	Teslas (SI)	10^{-4}
Magnetizing Force (H)	Oersteds (CGS)	Amperes per Meter (SI)	$1000/(4\pi)$

Table 3-3, Conversion Table (From Ref. [14]).

To determine the change in permeability versus dc bias, Figure (3-5) is entered along the horizontal axis using the magnetizing force determined from Equation (3-4). As is illustrated for the 147μ inductor at 43.25 Oersteds, the percent change in permeability can be as high as ≈ 50%. Such a change can significantly affect filter calculations where a decrease in permeability causes the inductance to decrease that in turn causes the cutoff frequency of the filter to increase. Appendix A contains the spec sheets for the inductor and Appendix B contains a MATLAB script file for inductance calculation.

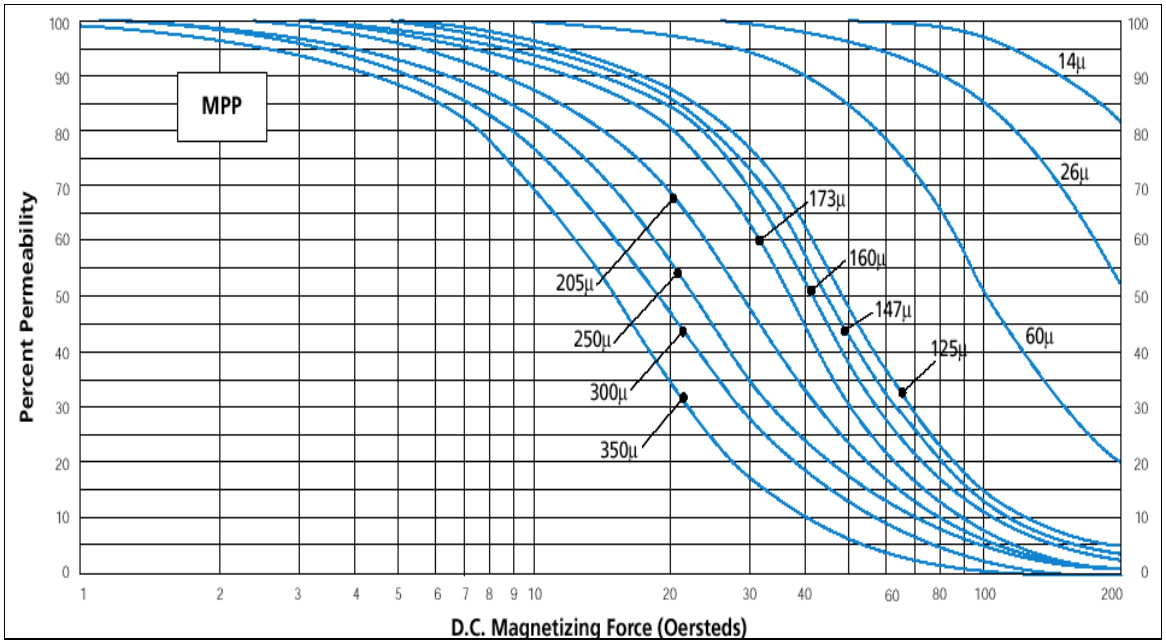


Figure 3-5, Percent Change in Permeability (From Ref. [14]).

To summarize the inductor design steps, the following is offered:

- determine duty cycle (D) from Equation (3-2),
- determine critical inductance (L_{crit}) from Equation (3-1),
- determine current (I), choose correct wire size from Table (3-2),
- calculate energy required (LI^2), enter graph and choose core weight from Figure (3-1),
- based on weight, select core from inductor catalog specification sheets Reference [14],
- calculate number of turns required (N) from Equation (3-3) and Reference [14],
- calculate magnetizing force (H) based on specs from specification sheet Reference [14] and Equation (3-4),
- calculate B_{max} based on data from specification sheet Reference [14] and Equations (3-4 through 3-7),
- calculate permeability (µ) from Equation (3-8) and Reference [14],
- enter B-H graphs in Reference [14] and Figure (3-4) and determine if inductor chosen is within the linear region,

- finally, determine percent change in permeability from Figure (3-5) and Reference [14].

Once the input filter frequency has been determined (L_{filter} and C_{filter}), the same steps listed above should be followed when deciding on a core for the input inductor.

2. Output Capacitor Sizing

Capacitor selection was based on parameters from Table (2-1) with buck chopper output voltage ripple (ΔV_c) less than 1% (4V peak-to-peak). To determine the correct capacitance, a full development from Reference [13] was utilized. From Reference [13], the difference between the maximum and minimum inductor current, I_{max}-I_{min}, is given by:

$$I_{max} - I_{min} = \frac{(E - V_c)}{L} \times DT \tag{3-9}$$

Substituting in the appropriate values, I_{max}-I_{min} = 4A. The change in charge (ΔQ) was calculated using Equation (3-10) with T = 50μsec, f = 20kHz:

$$\Delta Q = \frac{(I_{max} - I_{min})}{8} \times T \tag{3-10}$$

Substituting all values, ΔQ = 25μC. To find the minimum output capacitance required, Equation (2-4) was utilized and verified by Equations (3-11) and (3-12).

$$C = \frac{\Delta Q}{\Delta V_c} \tag{3-11}$$

$$\frac{\Delta V_c}{V_c} = \frac{T^2(1 - D)}{8LC} \tag{3-12}$$

Substituting all values into Equations (3-11) and (3-12) and assuming full load condition (L = 50% of theoretical value), C = 12.5μF, which is the minimum capacitance required. Note, capacitor selection is somewhat dependent on the dynamic response desired, for example, the requirement that there is enough energy to recover during a load transient. Equation (3-11) is only a steady-state requirement.

One must simulate the power section and control law to assess the appropriateness of capacitance selection. Reference [4] cited that actual capacitance required could range from 10 to 100 times C_{min}. A detailed buck chopper SIMULINK model was built and MATLAB m-files (used bessel pole locations) written to test various values of capacitance. Simulation revealed a capacitance of $\approx$500μF was required to obtain a reasonable transient response. The MATLAB script files and detailed SIMULINK model are contained in Appendix B.

Figure (3-6) illustrates two simulation runs, one for C = 50μF and one for C = 500μF. In each case, the control law feedback gains were modified to achieve identical closed-loop pole locations so that appropriate comparisons can be made (pole locations S = -2342.06 $\pm$j2234.30, -2959.38). The control law assumed is documented in Chapter IV. From the figure, it is apparent that C = 500μF is the more suitable choice for output capacitance. Figure (3-6) illustrates a step-change from minimum load (200Ω) to maximum load (20Ω) then a step change back to minimum load. For C = 50μF, the output voltage transient during both step changes is greater than 30V, motivating the choice of a larger capacitance value. For a similar load transients with C = 500μF, the output voltage remains within $\pm$4V. Values of capacitance much larger than 500μF introduce the possibility of large swings in the duty cycle during a transient, with the resulting rail-to-rail signal injecting spurious noise into the system. A 500μF output capacitance was deemed adequate in terms of transient response and duty cycle performance.

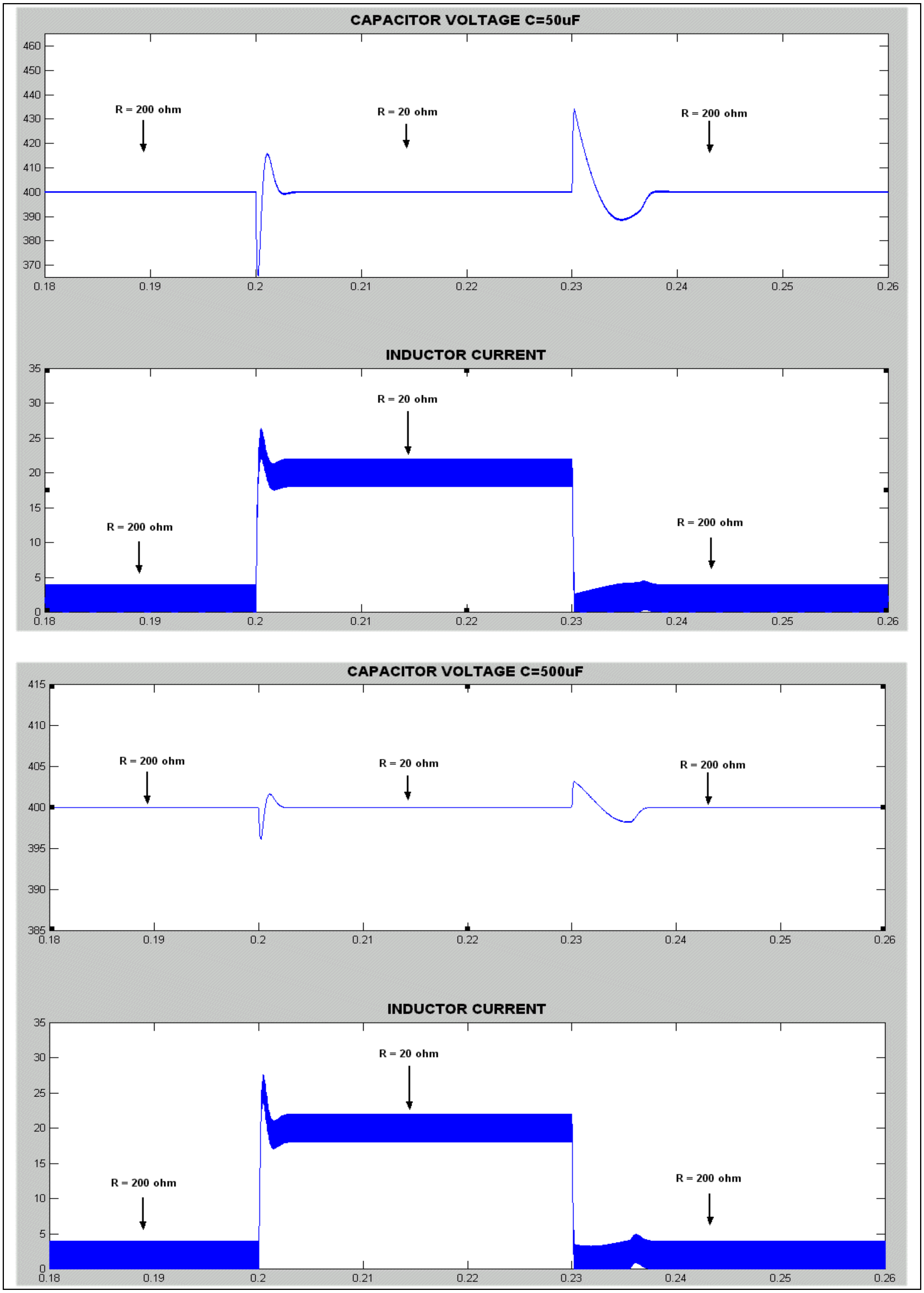


Figure 3-6, Output Voltage and Power Section Inductor Current Plots.

Care must be exercised when selecting the proper capacitor. In general, the specification sheet will list maximum ripple current and frequency response. For this project, a capacitor with $6A_{rms}$ (from spec sheet) ripple at 20kHz was selected to ensure components were within specification guidelines. The capacitor spec sheet is included in Appendix A.

3. Input Filter Selection

The input filter, illustrated in Figure (2-1), must allow the 360Hz ripple from the assumed six-pulse rectifier to pass and to ensure that the switching frequency from the main switch is blocked. Blocking the switching frequency ensures that the IGBT switching action will not be fed back to other converters supplied by the same rectifier.

To determine filter capacitor and inductor size, the resonant peak of the filter was chosen to be 450Hz. This resonant frequency allowed 360Hz to pass and was at least one decade below the switching frequency of the IGBT prohibiting it from affecting the input. Substituting into Equation (3-13) with f_o = 450Hz and C = 500μF (selected for its availability in the lab), L was determined to be 250μH.

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{3-13}$$

Referring back to Figure (3-5), the inductor permeability could change as much as fifty-percent thus decreasing inductance as much as fifty percent. Taking the aforementioned into account and following the same procedures listed above for the buck chopper power section inductor, the input filter inductor was hand wound (55 turns) for 0.4mH and measured 0.357mH in the lab using the same test equipment as previously mentioned.

Concern lied in the dc bias portion of the circuit. From specifications listed in Table (2-1), P_{out} = 8kW and V_{in} = E = $500V_{dc}$. Noting that for an ideal converter $P_{in} = P_{out} = V_{in}^2/R$ and solving for R reveals that the filter "sees" a steady-state impedance of 31.25Ω (Note, a more detailed analysis is required to characterize the incremental small-

signal input impedance). With I = E/R, 16A of dc bias is going through the inductor as shown from the PSPICE simulation in Figure (3-7). As in the case of the power section inductor, the permeability of the filter inductor will change with an increase in dc-bias. Entering Equation (3-4), where N = 55, I = 16A and l_e = 25cm, H $\approx$ 44.2 Oersteds. Next, entering Figure (3-5) it is seen that the permeability can change as much as $\approx$ 85%, resulting in a worst-case $f_{cutoff} \approx 968.5$Hz. The increase in the cutoff frequency is not an issue since the 360 Hz will pass while 20kHz is blocked. The specification sheets are contained in Appendix A and Reference [14].

Illustrated in Figure (3-7), Rf1 through Rf3 function to provide appreciable damping at the LC resonant frequency [13]. From [13], $Rf = \sqrt{L/C}$ where L = 357µH and C = 500µF which results in $Rf \approx 0.84\Omega$. High wattage (2W) resistors were available in the lab; therefore, 3-3Ω resistors were placed in parallel to achieve $\approx$ 1Ω of dampening resistance, close to the theoretical value of 0.84Ω. Finally, the 45µF capacitor in Figure (3-7) provided additional damping (found experimentally). No calculations were used to select the 45µF capacitor, it was available in the lab and its capacitance had a minimal impact on total capacitance in the input filter.

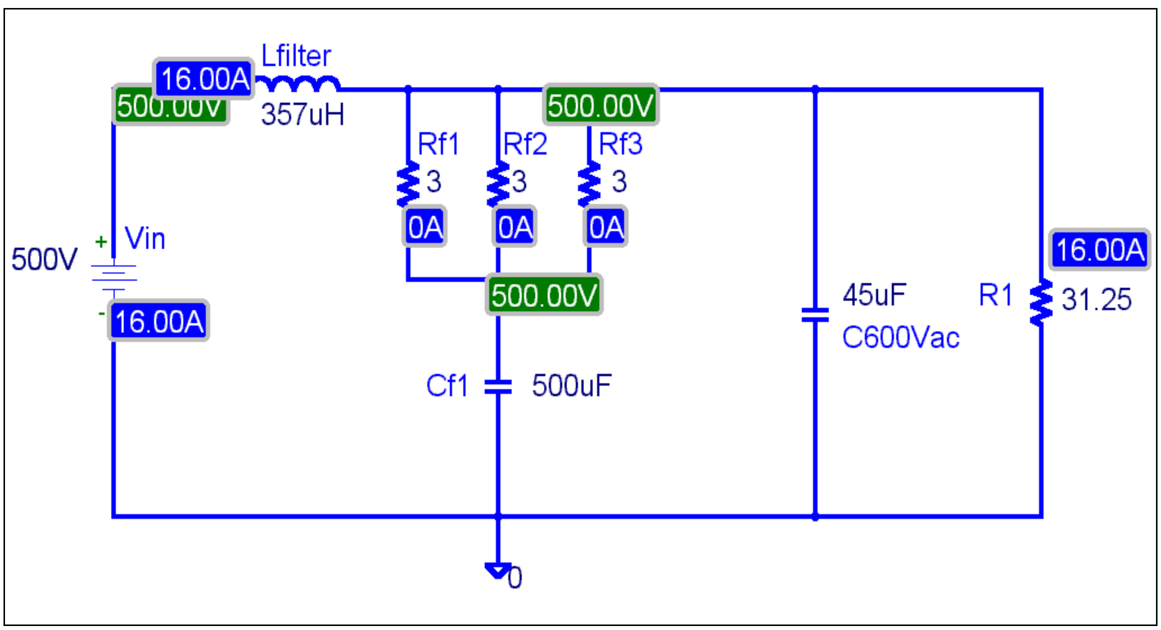


Figure 3-7, Buck Converter Input Filter.

Simulation was conducted on the circuit in Figure (3-7) using Multisim software from Electronic Workbench. Figure (3-8) illustrates the bode plot for the ideal low-pass filter. The cursor indicates that the response begins to roll off near ≈ 440Hz, which was acceptable for this design.

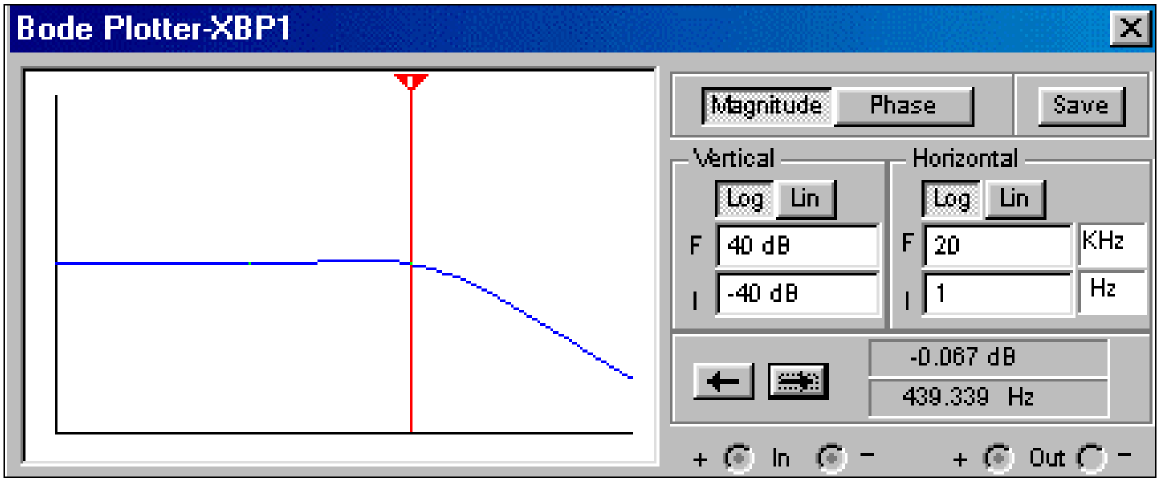


Figure 3-8, Bode Plot Input Filter.

4. Current Sensors

In Chapter IV, the analog control board and current sensing boards are discussed in detail and Easytrax layouts are provided in Appendix D. The feedback control law utilizes measurements of the output current (i_o) and the power section inductor current (i_L). In Figure (3-9), two inputs to the control board are labeled $i_o/5$ and $i_L/5$. (Note, circuit labeling conventions are addressed in Chapter V). These inputs are obtained from the CLN-50 Hall-effect current sensor from manufacturer F.W. Bell. Appendix A contains data sheets for the CLN-50.

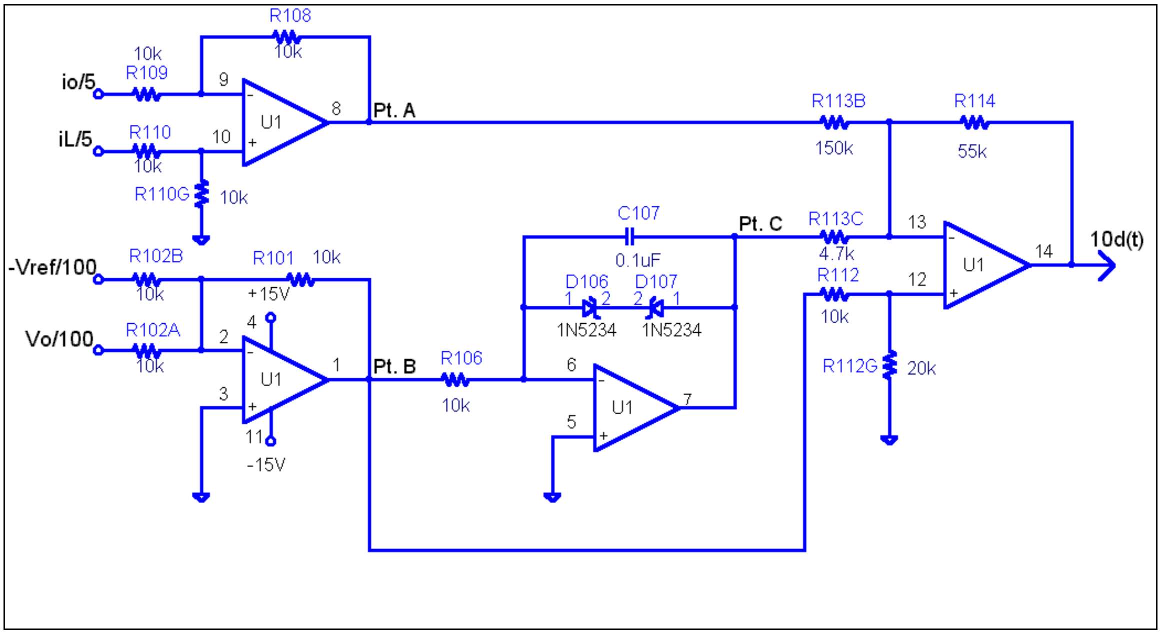


Figure 3-9, Control Circuit Inputs.

The CLN-50 accurately measures dc and ac current and provides electrical isolation between the current-carrying conductor and the output of the sensor. The current sensor uses the Hall effect to sense the magnetic field and output a proportional voltage. The Hall effect is defined as follows: If a conductor carrying a current (I) is placed in a magnetic field of density (B) in a direction normal to it, then an electric field, and therefore a potential, is set up across the width of the conductor. This is the Hall effect, the generation of an electromotive force (e.m.f.) by the movement of electrons through a magnetic field. The Hall e.m.f. is picked off by tappings applied to the conductor edge for the measurement of current.

The current-carrying conductor placed through the window of the CLN-50 produces a magnetic field that is proportional to the current. The current through the coil produces an opposing field to that provided by the current through the aperture; therefore, flux in the core is constantly driven to zero. The coil is connected to the output of the sensor and the output is a current proportional to the aperture current multiplied by the number of turns of the coil. This project utilized 1000-turn coils providing 1mA of output current for 1A of circuit current. The output current is converted to a voltage by connecting the output current through a resistor (200Ω). The resulting voltage signal out

of the sensor is equal to the circuit current divided by five. This signal is then fed to the control board as discussed in Chapter IV. A different scaling can be achieved by adjusting the resistor value.

According to Reference [18], Hall-effect sensors provide an advantage over traditional resistive shunt and current transformer methods in that the Hall-effect can both measure ac and dc current and provide electrical isolation. Hall-effect sensors also offer the following:

- low cost method of measuring larger ac and dc currents,
- high frequency range (>150kHz, not applicable to this design),
- no magnetic hysteresis or offset,
- fast response and excellent linearity,
- several sensors can be connected in parallel to the same supply.

Finally, to achieve the most accurate reading from the sensor, the wire was placed as close as possible to the center of the aperture. Furthermore, to avoid interference from other large current-carrying conductors in the buck converter module, sensors were carefully located in the buck converter enclosure (location illustrated in Chapter V).

5. Pulsed Width Modulation Chip Selection (UC3637)

Figure (3-10) illustrates the Pulse Width Modulation (PWM) stage. This circuit is comprised of the UC3637 chip by Unitrode. Data sheets are included in Appendix A and design considerations with applicable equations are discussed in Reference [19]. The UC3637 is available in industrial and military grades (UC2637 and UC1637, respectively).

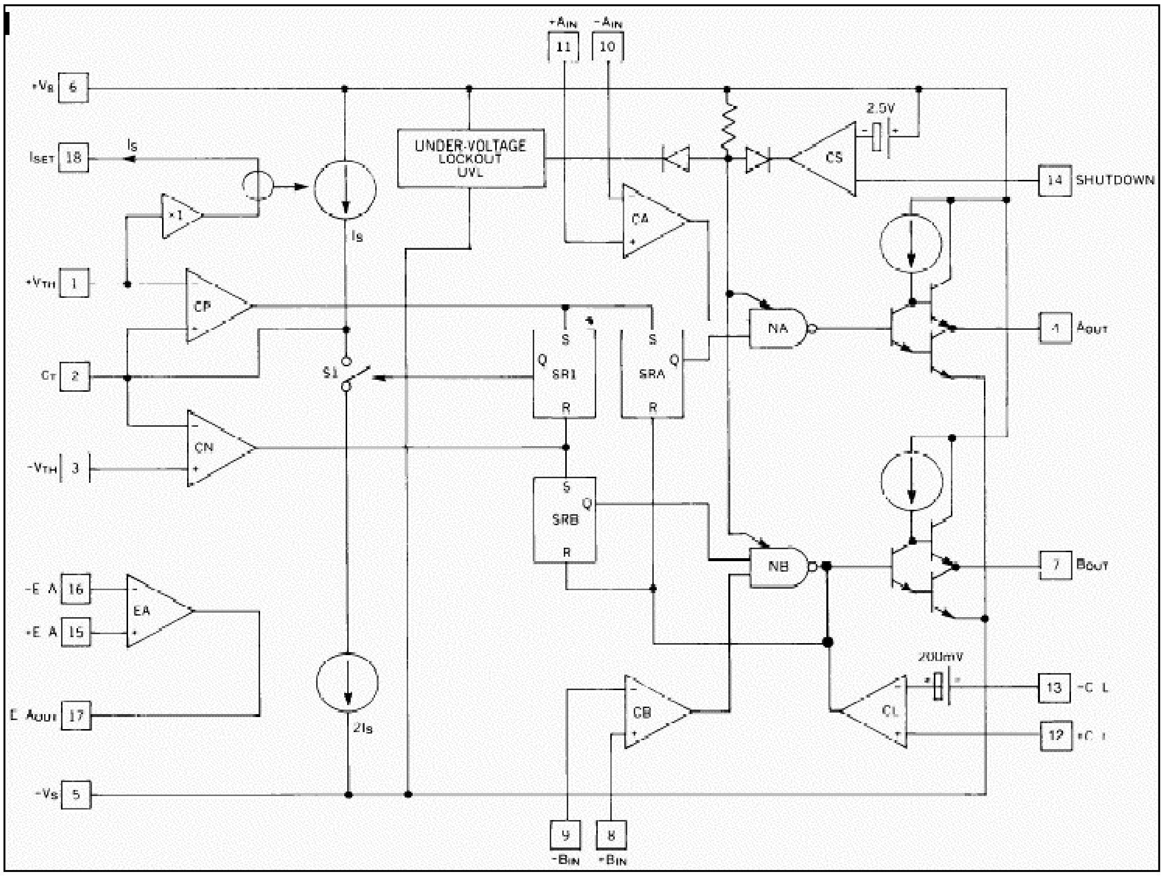


Figure 3-10, Block Diagram of UC3637 (From Ref. [19]).

The UC3637 implements pulse width modulation. PWM is basically a switching technique where the supply voltage is applied to the load and then removed. The on times and off times are controlled as precisely as possible. The main function is to regulate the flow of energy from a power supply to a load, under the control of an input signal.

Figure (3-10) is a block diagram of the UC3637. Reference [19] discusses in detail the functional operation of each sub-block and defines all abbreviations (i.e. CP, CN). The main functions discussed in Reference [19] are:

- triangle wave generator; CP, CN, S1, SR1,
- PWM comparators; CA, CB,
- output control gates; NA, NB,
- current limit; CL, SRA, SRB,

- error amplifier; EA,
- shutdown comparator; CS,
- and undervoltage lockout; UVL.

Ratings for the device are included in Appendix A.

The UC3637 receives the analog duty cycle 10d(t) (0-10V), from the main control circuit, discussed in Chapter IV, and produces a square wave output at a frequency of ≈20.4kHz. Charging capacitor, C_{302} in Figure (3-11), generates the triangle wave. C_{302} was calculated using Equations (3-14) and (3-15).

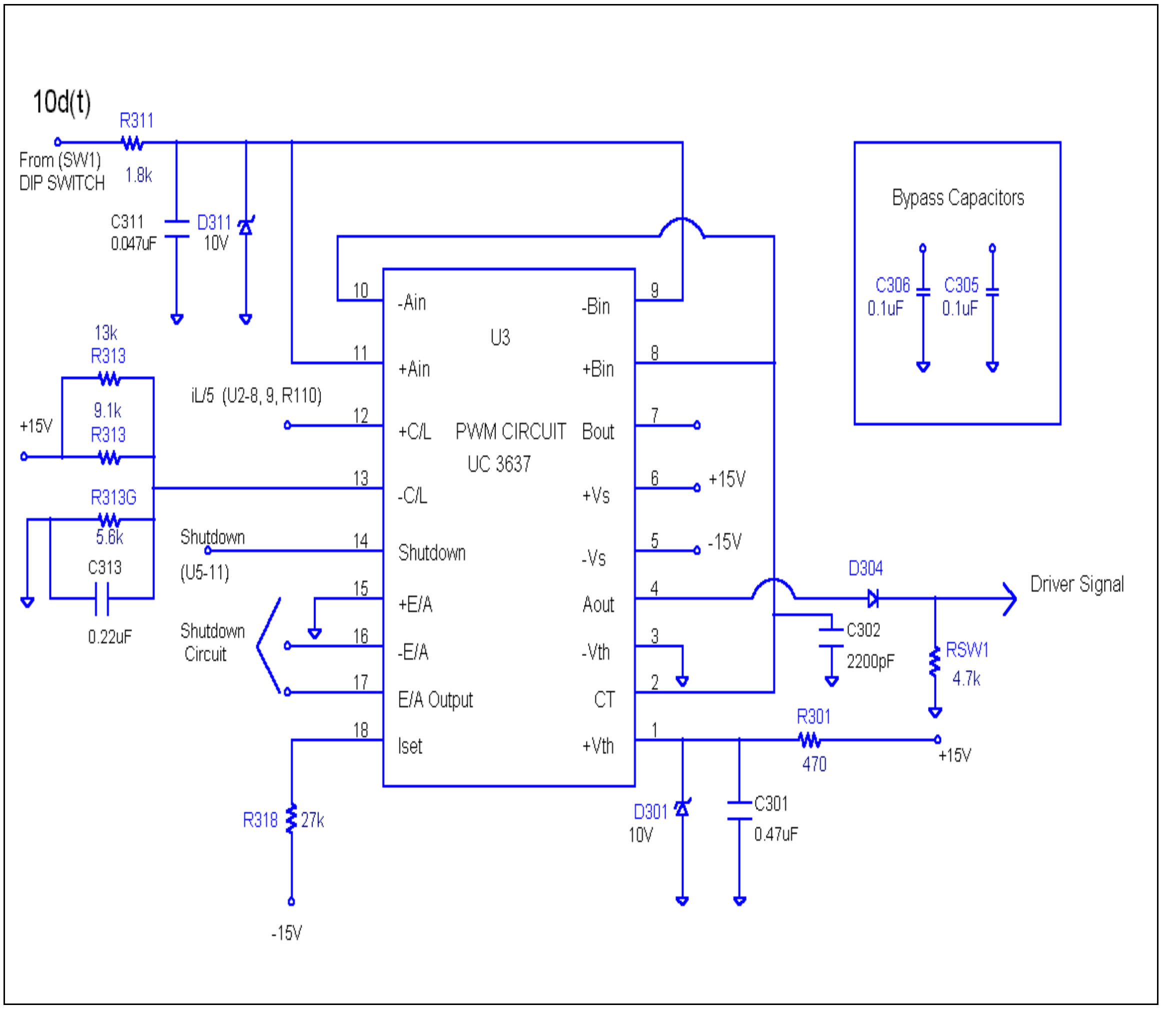


Figure 3-11, PWM Circuit Diagram.

$$I_S = \frac{(+V_{TH}) - (-V_S)}{R_{318}} \tag{3-14}$$

$$f = \frac{I_S}{2 \times C_{302}\left[(+V_{TH}) - (-V_{TH})\right]} \tag{3-15}$$

In the previous equations, I_S is the current through R_{318}, $+V_{TH}$ is the upper threshold voltage (10V), $-V_{TH}$ is the lower threshold voltage (0V), f is the frequency (20kHz desired), and V_S is the supply voltage ($\pm$15V). Choosing R_{318} = 27kΩ, $I_S \approx$ 0.0009mA. Solving Equation (3-15), through iterative process, C_{302} was $\approx$2200pF, which yielded a frequency of $\approx$ 20.4kHz. From the PWM stage, the driver pulse (see Figure 3-11) is sent via pin four of the UC3637 to the IGBT driver board discussed in Chapter IV. It should be noted that the threshold voltages were user selected to meet the 0-10V output capability of a standard D/A chip.

6. IGBT Selection

Selection of the proper IGBT was based on the specifications listed in Table (2-1) and the lead-time specified by the manufacturer. To meet specs and project deadline, Semikron SKM100GB124D IGBT was selected. The device is rated for 1200V/100A at 20kHz, well within design requirements. The IGBT already includes a fast recovery diode as part of the module; therefore, an external fast recovery diode is not required. Appendix A contains the data sheets for the IGBT.

C. SUMMARY

This chapter focused on the process of selecting major components for the prototype SSCM. Appendix C contains the parts list used in the design along with expected lead times and price information as of April 2001 (for major components only). With the major components introduced, the design of the main control circuit, sensor boards, and the IGBT driver board are detailed next. The equations implemented by the

control board and the operations of the commercially-available IGBT driver board are documented in Chapter IV.

IV. CONTROL BOARD AND SUPPORTING CIRCUITS DESIGN

A. FEEDBACK CONTROL OF THE BUCK CHOPPER

The purpose the buck chopper feedback control is to establish suitable voltage regulation. For testing the converter, the converter output must remain nearly constant under changing load and input conditions. Switching functions must adjust to maintain nearly precise operation, and adjustment must be performed whenever the converter operates. As addressed in Reference [20], practical power converters do not provide adequate open-loop regulation. Most open-loop controlled converters produce an output dependent on the input, and do not provide inherent line regulation. At low power, the effects of equivalent series resistance (ESR), voltage drops across semiconductor switches, and even wire resistance make operation load dependent. To account for these effects, the duty ratio of a dc-dc converter must be altered and made a function of the output.

A system is said to be asymptotically stable if it returns to the original operating conditions after being altered or disturbed. In general, control can be achieved via open-loop or closed-loop techniques. With open-loop control, the duty cycle is set without information about the system state and no corrective action can take place if a disturbance occurs. With this in mind, it is apparent that closing the loop is vital if proper regulation and stability are to be maintained in the dc-dc converter. Stability is required for small, fast disturbances such as noise, for large disturbances such as startup or loss of load, and for periodic disturbances such as input ripple. As stated in Chapter II, the dc-dc converter control must be robust; hence, the control circuitry must be robust.

Closed-loop or negative feedback control makes a measurement of the output and compares this signal to the desired signal. An error signal is developed and the control input is altered to account for this error. Closed-loop control can offer undesirable results as well. The error signal is intended to be zero; however, if zero error is developed there will be no error signal to drive the control parameter. As will be seen in a later section, to alleviate this problem, integral control was utilized since the integrator

produces nonzero output even when the input is zero. It should be mentioned that care must be exercised when choosing gains or the integral control could result in instability. The purpose of this chapter is to develop the control equations and explain the control circuitry utilized in the design.

B. ANALOG CONTROL BOARD

1. Main Control Stage Circuit Equations

Control for the buck chopper was accomplished utilizing the analog control algorithm adapted from Reference [21] and described in Equation (4-1). Appropriate Bessel pole locations are selected and feedback gains derived using MATLAB code documented in Appendix B. The main control circuitry, illustrated in Figure (4-1), implements the algorithm given in Equation (4-1).

$$d(t) = -h_v\left(v_{out} - v_{ref}\right) - h_n \int \left(v_{out} - v_{ref}\right) dt - h_i\left(i_L - i_{out}\right) \qquad (4\text{-}1)$$

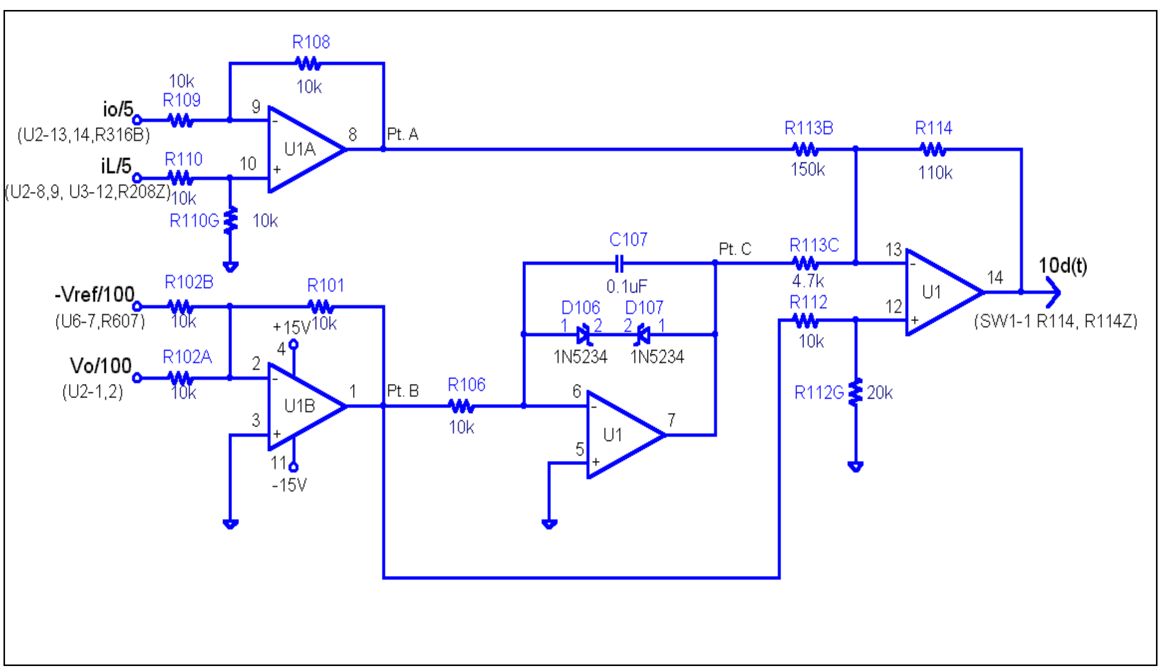


Figure 4-1, Main Control Stage (After Ref. [10]).

Equation (4-1) states that the duty cycle perturbations are a function of the output voltage, the inductor current, and the output current. With the control loop speed slower than the switching frequency (20kHz), one may view the switching frequency harmonics as being filtered out and that the duty cycle is a function of the averaged values of the circuit variables. From Equation (4-1), d(t) is the duty cycle, h_v is the proportional voltage gain, h_n is the integral voltage gain, and h_i is the proportional capacitor current gain. The term $h_i(i_L-i_{out})$ essentially implements the feedback of the derivative of the output voltage. By selecting the proper feedback gains h_i, h_n, and h_v, the desired closed-loop response can be obtained.

As illustrated in Figure (4-1) and included in Equation (4-1), both current and voltage feedback were utilized. Without current feedback, the transient response of the converter is slow, since changes in the duty cycle would only take place with a perturbation in the output voltage (V_{out}). Thus, rapid output current changes (step changes for instance) introduce near-instantaneous modifications to the switch duty cycle.

Before pole placement was resolved, a closed-loop transfer function for the buck chopper and control was determined. The closed-loop system is illustrated in Figure (4-2). The upper right hand block was derived for the buck chopper (the plant) in References [10] and [13].

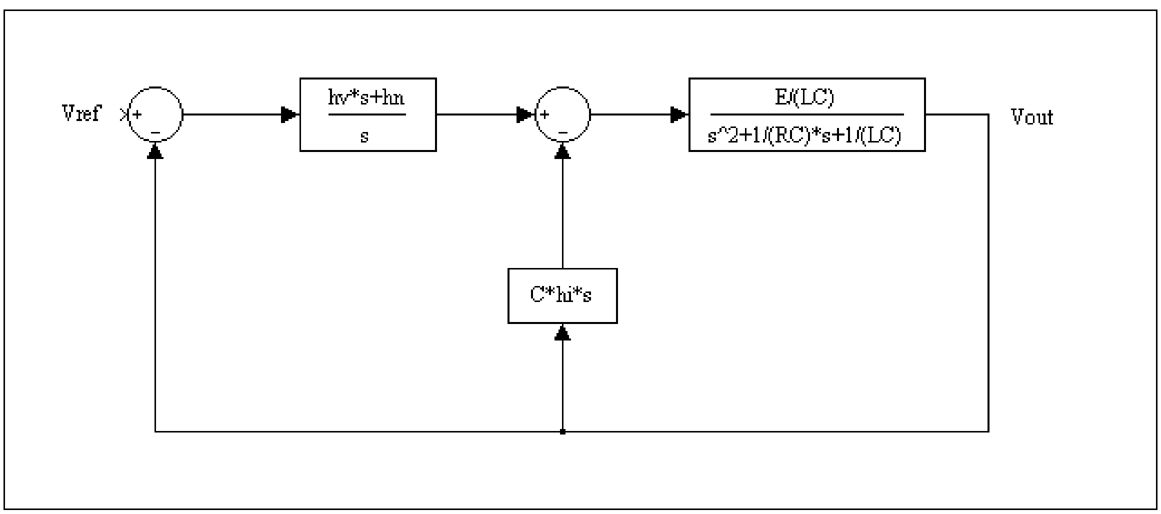


Figure 4-2, Buck Converter Closed-Loop System.

Solving the closed-loop transfer function resulted in Equation (4-2) where E, L, C, and R are known constants listed in Chapters II and III.

$$\frac{v_{out}}{v_{ref}} = \frac{\frac{E}{LC}(h_v s + h_n)}{s^3 + \left(\frac{1}{RC} + \frac{E}{L} \times h_i\right)s^2 + \left(\frac{1}{LC} + \frac{E}{LC} \times h_v\right)s + \frac{E}{LC} \times h_n} \tag{4-2}$$

By writing the nodal equations applicable to Figure (4-1), labeled Pt A, Pt B, Pt C, and 10d(t), equations for the unknown gains (h_v, h_n, h_i) can be obtained. Referring to points A, B, C, and d(t) in Figure (4-1), Equations (4-3) through (4-9) follow. At point A (note, circuit labeling conventions are addressed in Chapter V):

$$A = \frac{-R_{108}}{R_{109}}\left(\frac{i_o}{5}\right) + \frac{R_{110G}}{R_{110} + R_{110G}}\left(1 + \frac{R_{108}}{R_{109}}\right) \times \frac{i_L}{5} \tag{4-3}$$

Arbitrarily choosing the same resistor values for U1A and U1B and realizing from Figure (1-4) that capacitor current is $i_C = i_L - i_o$, Equation (4-3) simplifies to Equation (4-4).

$$A = \frac{1}{5}(i_C) \tag{4-4}$$

At point B:

$$B = \frac{-R_{101}}{R_{102B}}\left(\frac{-V_{ref}}{100}\right) - \left(\frac{R_{101}}{R_{102A}}\right) \times \left(\frac{V_o}{100}\right) \tag{4-5}$$

Substituting the designated resistor values for these op-amps results in Equation (4-6).

$$B = -\frac{1}{100}(V_o - V_{ref}) \tag{4-6}$$

Continuing, the evaluation at point C yields Equation (4-7).

$$C = \frac{1}{100 \times C_{107} R_{106}} \int \left(V_o - V_{ref} \right) dt \tag{4-7}$$

Zener diodes, D_{106} and D_{107}, connected to U1C prevent integrator windup. These diodes function to clamp the integrator and prevent an unlimited buildup of voltage (zener breakdown voltage is 6.2V).

Finally, writing the equation at 10d(t) yields Equation (4-8) and after some algebraic manipulation, Equation (4-9) results.

$$10d(t) = \frac{-R_{114}}{R_{113B}}(A) - \frac{R_{114}}{R_{113C}}(C) + \frac{R_{112G}}{R_{112}+R_{112G}}\left(1 + \frac{R_{114}}{R_{113B} \,//\, R_{113C}}\right)(B) \tag{4-8}$$

$$\begin{gathered} 10d(t) = \frac{-R_{114}}{5R_{113B}}(i_C) - \frac{R_{114}}{100 R_{113C} C_{107} R_{106}} \int \left(V_o - V_{ref} \right) dt - \\ \left[\frac{1}{100} \left(\frac{R_{112G}}{R_{112}+R_{112G}} \right) \left(1 + \frac{R_{114}}{R_{113B} \,//\, R_{113C}} \right) \right] (V_o - V_{ref}) \end{gathered} \tag{4-9}$$

Revisiting Equation (4-1), it is apparent from Equation (4-9), after dividing through by ten, that the coefficient of capacitor current (i_C) is h_i, the coefficient for the integral term is h_n, and the coefficient for the voltage error (V_o-V_{ref}) is h_v resulting in Equations (4-10) through (4-12).

$$h_i = \frac{R_{114}}{50 R_{113B}} \tag{4-10}$$

$$h_n = \frac{R_{114}}{1000 R_{113C} C_{107} R_{106}} \tag{4-11}$$

$$h_v = \frac{1}{1000}\left(\frac{R_{112G}}{R_{112}+R_{112G}}\right)\left(1+\frac{R_{114}}{R_{113B} \mathbin{//} R_{113C}}\right) \tag{4-12}$$

From Equations (4-10) through (4-12), it is apparent that once the gains are resolved resistor values for U1C and U1D in Figure (4-1) can be determined.

2. Pole Placement and Gain Selection

There are uncountable alternatives for pole-placement design. In general, the design should produce poles with roughly equal (and high) magnitudes, spread along an arc in the left-half complex (s) plane. Imaginary parts should not be larger than real parts for any pole [20].

To minimize the control gains a Bessel function polynomial approximation was utilized [22]. The pole locations are listed in Table (4-1), and the multiplication factor, (ω), is 2π500. To prevent unwanted controller actions, ω must be sized at least one decade below the radian switching frequency (2π*20kHz). In general, the selection of ω should not require excessive duty cycle control effort, which introduces unwanted noise in the controller [21].

Pole	**Location**
S_1	-0.7455ω + j0.7112ω
S_2	-0.7455ω - j0.7112ω
S_3	-0.9420ω

Table 4-1, Bessel Pole Locations.

Expanding the pole locations from Table (4-1) into a third-order polynomial yields Equation (4-13), which further simplifies to Equation (4-14).

$$(S+0.7455\omega-j0.7112\omega)(S+0.7455\omega+j0.7112\omega)(S+0.9420\omega) \tag{4-13}$$

$$S^3 + 7643.5S^2 + 2.43 \times 10^7 S + 3.10 \times 10^{10} \qquad (4\text{-}14)$$

Next, the (S) coefficients from the denominator of Equation (4-2) and the (S) coefficients from Equation (4-14) were equated resulting in the gains listed in Table (4-2). These gains were determined using E = 500V, L = 1mH, C = 500μF, and R = 200Ω.

Closed-Loop Pole Locations	$S = -2342.06 \pm j2234.30, -2959.38$
Proportional Voltage Gain	$h_v = 0.017$
Proportional Current Gain	$h_i = 0.015$
Integral Voltage Gain	$h_n = 23.40$

Table 4-2, Buck Converter Closed-Loop Poles and Gains.

Substituting the gains listed in Table (4-2) into Equations (4-10) through (4-12) allows calculation of the remaining resistor values for Figure (4-1). It should be noted that the following was assumed when carrying out the calculations for the final resistor values:

- U1A and U1B were assumed unity gain,
- R_{113B}, C_{107}, R_{112G}, R_{106} in Figure (4-1) were arbitrarily chosen.

The derivation just described was for 100% loading. To ensure the system maintains stable operation, pole locations must be reassessed throughout the entire load range. Although many combinations of resistors could have achieved the desired results, this project kept resistor values between 2kΩ and 200kΩ. The resistor values were kept above 2kΩ to ensure that op-amp current limit was not exceeded while values were kept below 200kΩ to minimize noise from Electro-Magnetic Interference (EMI) and prevent interaction with op-amp input impedance. Appendix B contains the MATLAB code utilized to solve for the unknown gains and remaining resistor values.

3. Main Control Stage Stability

To pictorially verify the stability of the control system, the rise time, settling time, steady-state error, and the overshoot were investigated. Reference [23] defines the

preceding terms. Rise time is the time required for the step response to rise from 10% to 90% of its final value. Settling time is the time required for the system output to settle within a certain percentage of the nominal output. Steady-state error is the error when the time period is large and the transient response has decayed, leaving the continuous response. Finally, overshoot characterizes the amount the output swings past the steady-state output for a given step input.

The stability of the control system was verified using MATLAB. The open-loop frequency response was first investigated followed by the closed-loop response.

Open-loop response for R_{load} equal to 20Ω is illustrated at the top of Figure (4-3) while R_{load} equal to 200Ω is pictured at the bottom of Figure (4-3).

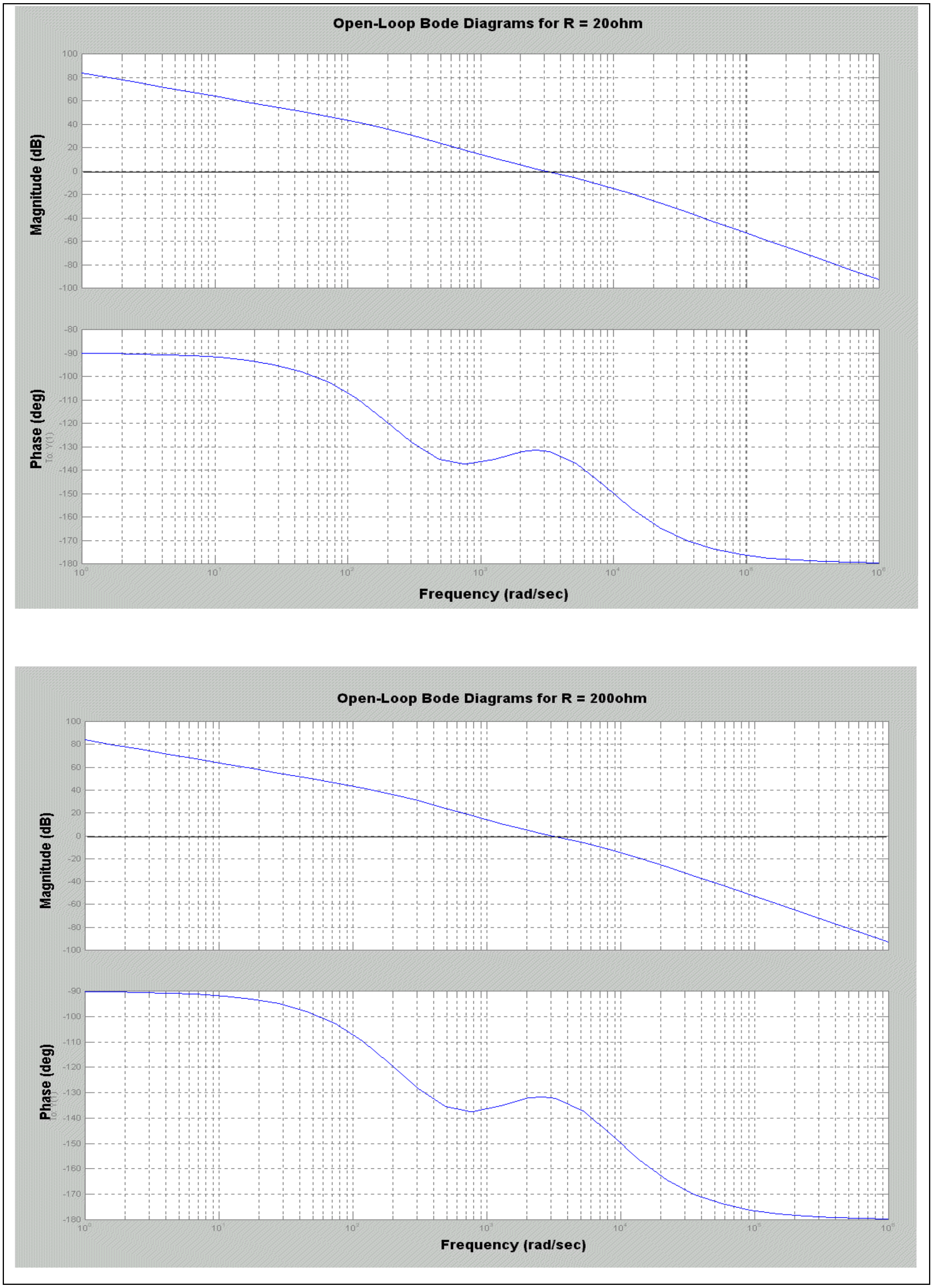
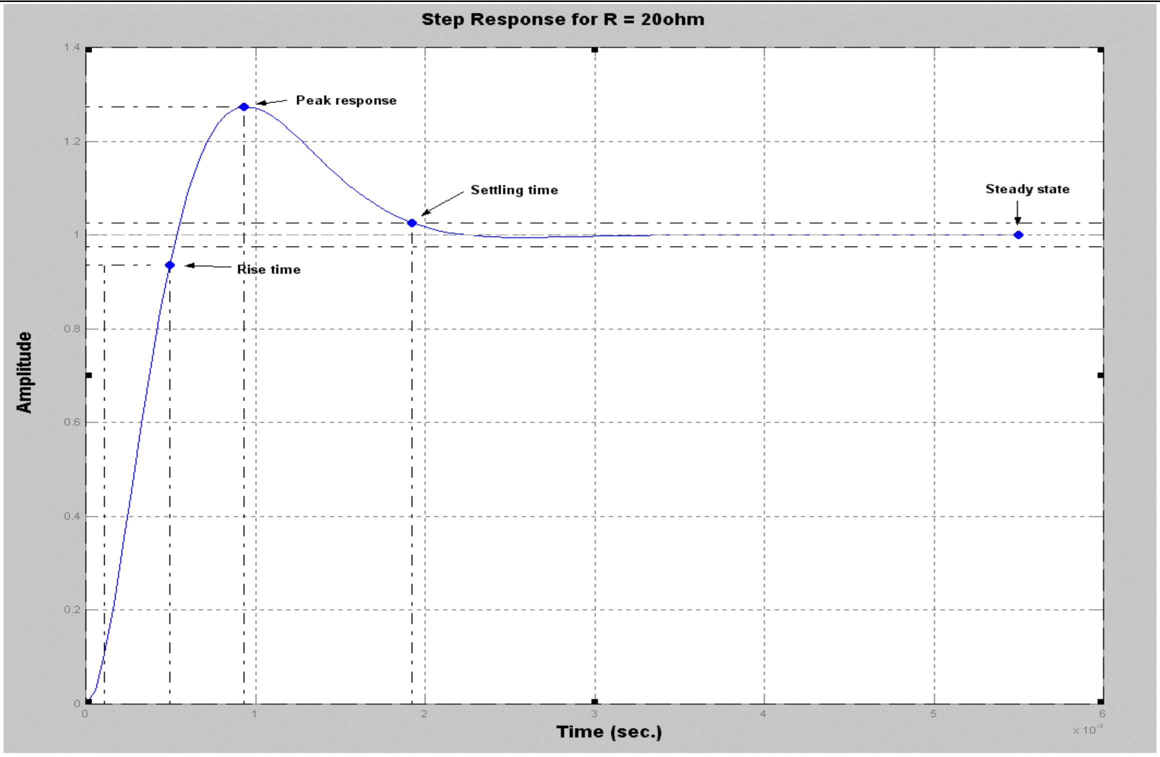


Figure 4-3, Open-Loop Frequency Response for 100% and 10% Load.

The crossover frequency in Figure (4-3) is the frequency at which open-loop gain is 0dB. Phase margin (PM) is 180° minus the phase of the transfer function at the crossover frequency ($PM \approx 48°$ in Figure (4-3)). The gain margin (GM) is the inverse of the open-loop gain magnitude at the frequency where the phase is 180° ($GM \geq 95dB$ in Figure (4-3)). As illustrated in Figure (4-3) with both PM > 0 and GM > 0, the system is stable.

Next, the closed-loop step response (for a change in V_{ref}) and Bode plots for R_{load} equal to 20Ω (100% load) are illustrated in Figure (4-4). The top plot is the step response showing the rise time, settling time, peak response, and the time to reach steady state. MATLAB contains a graphical function that will allow all these points to automatically be annotated on the plot. Appendix B contains the MATLAB code to generate the illustrated plots.



(Note, time scale in figure is multiplied by 10^{-3})

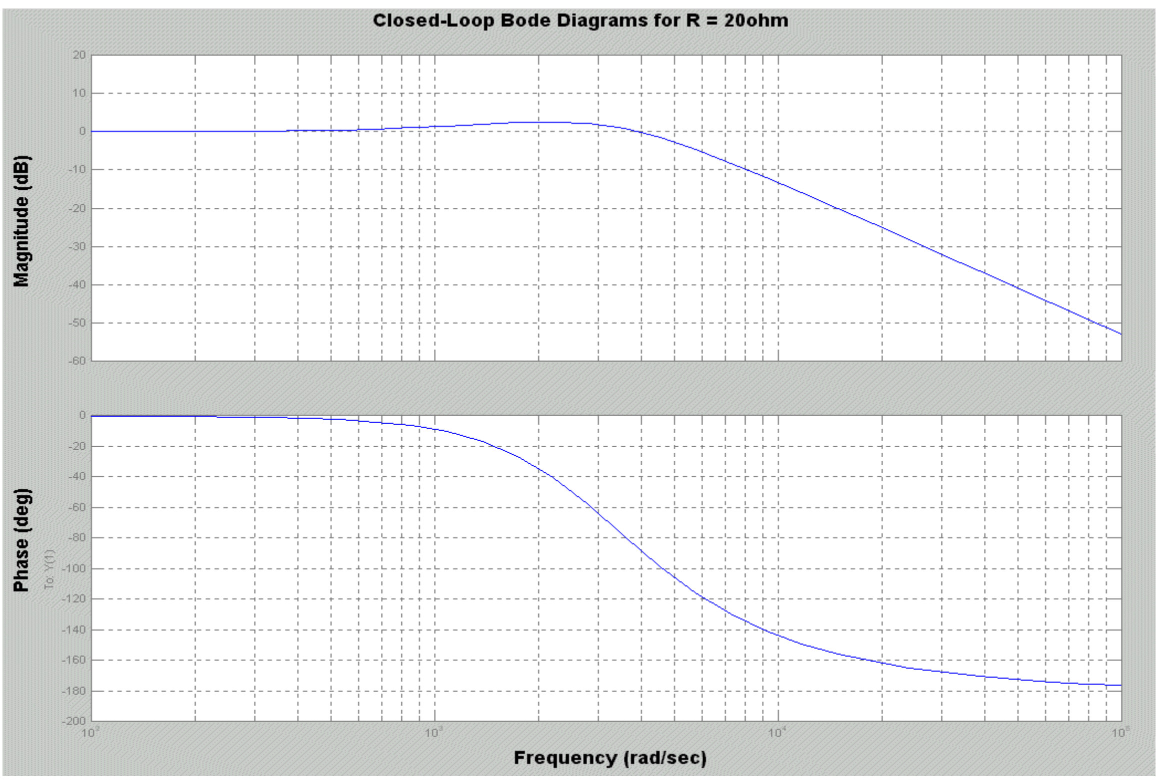
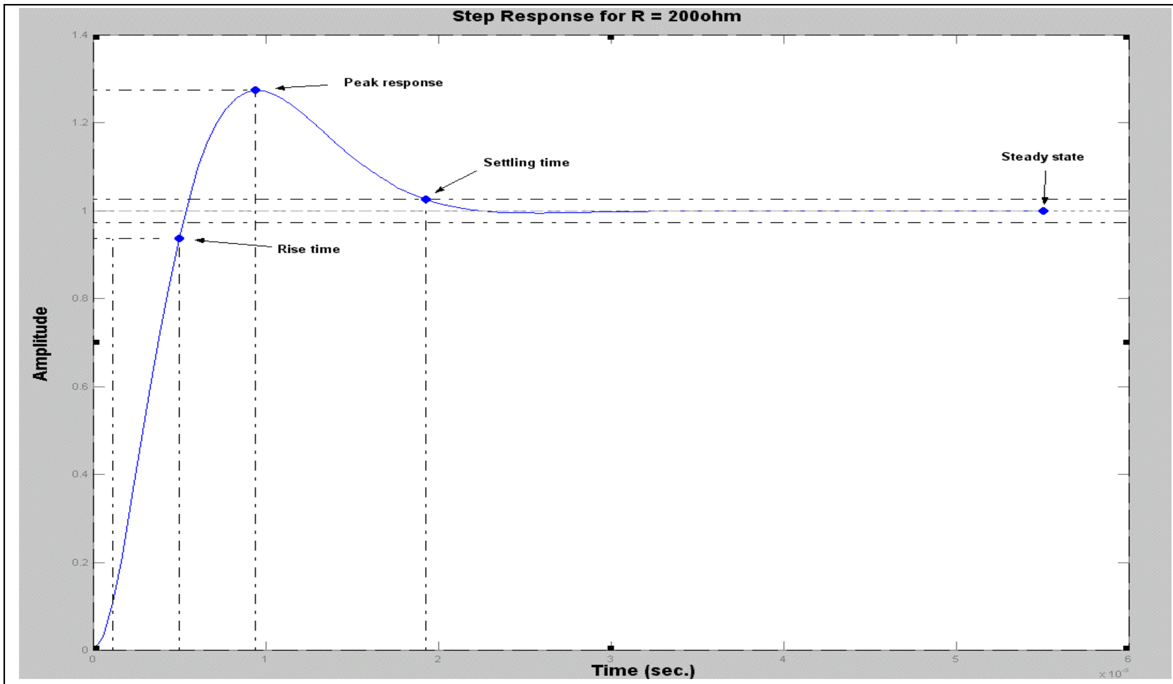


Figure 4-4, Step Response and Closed-Loop Frequency Response 100% Load.

The step response and bode plots for R_{load} equal to 200Ω (10% load) are illustrated in Figure (4-5).



(Note, time scale in figure is multiplied by 10^{-3})

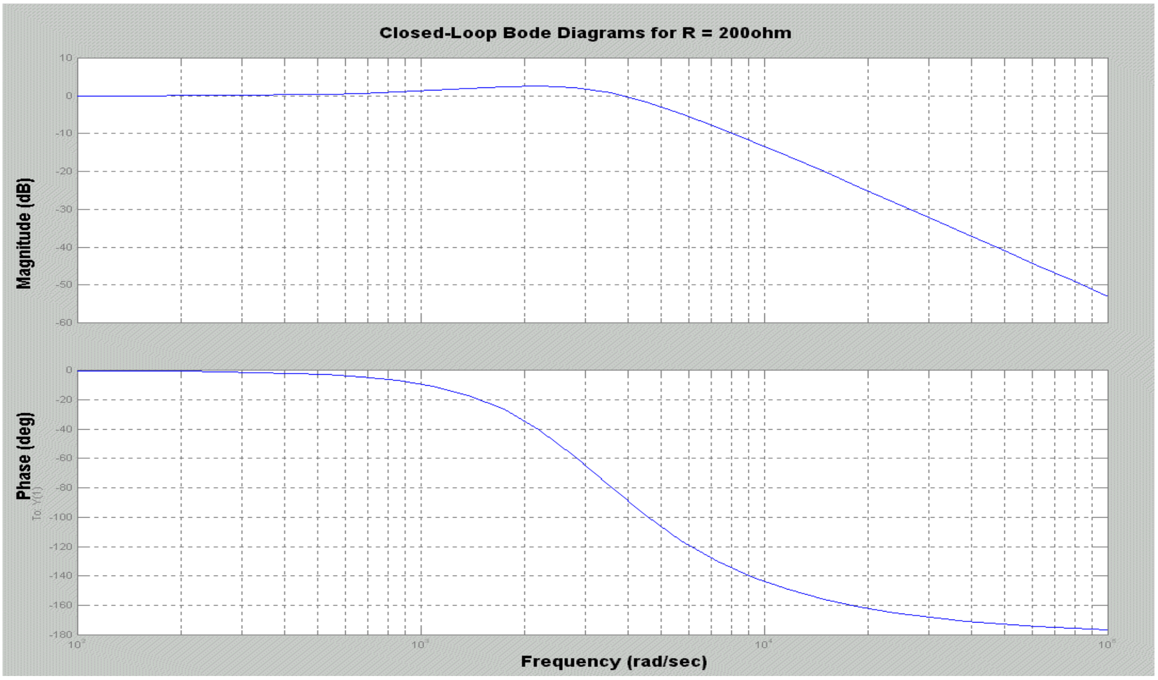


Figure 4-5, Step Response and Closed-Loop Frequency Response 10% Load.

As can be determined from Figures (4-4 and 4-5), the control loop system is stable throughout the entire load range. LF347 Texas Instrument quad operational amplifier was utilized to realize the control loop circuitry illustrated in Figure (4-1). Data sheets for this particular chip are contained in Appendix A. The output of the control stage 10d(t) is fed to the UC3637 PWM chip as indicated in Figures (3-9 and 3-11).

C. IGBT DRIVER BOARD SELECTION

The IGBT Driver Board is fully described and illustrated in Appendix A. A Semikron SKHI 10/17 High Power Single IGBT Driver meets specification requirements listed in Table (2-1) and was selected for this design. This driver is capable of switching up to a 400A IGBT module at 20kHz, which meets or exceeds design requirements

The driver includes a user input voltage level selector (+15V or +5V). For this design +15V was selected because all control circuitry utilized $\pm$15V; however, the card is capable of TTL input operation. As outlined in Appendix A, the +5V logic can be realized by bridging the pads marked "J1" together. For long input cabling, greater than 50cm, +15V is recommended due to EMI considerations.

A simple test circuit was set up in the lab to test the driver prior to full circuit interface. Figure (4-6) illustrates the required connections and Appendix A contains the detailed testing procedure.

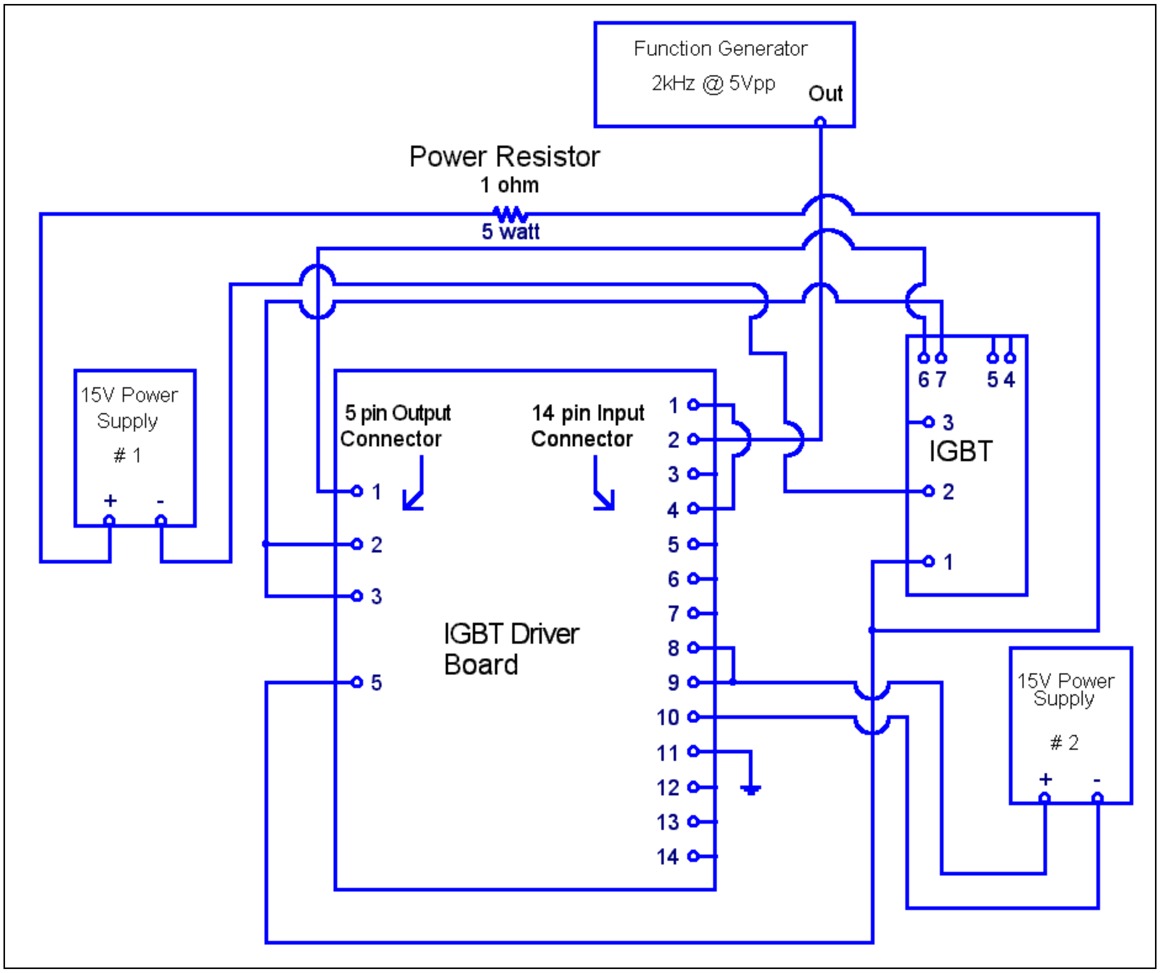


Figure 4-6, IGBT Driver Board Test Circuit.

Waveforms were monitored on two oscilloscope channels. Channel two was set up across the power resistor to monitor the performance of the IGBT, while channel one monitored the function generator and was set up between pin 2 and pin 11 of the IGBT driver board input connector. All other performance checks were followed as outlined in Appendix A.

In Figure (4-6), the IGBT driver board receives its input on pin two of the input connector (14-pin connector). In Figure (4-6), the function generator is feeding pin 2 for test purposes only. In actual circuit interface, pin 2 receives its input from the PWM chip pin 4, which is labeled A_{out} in Figure (3-10). The output of the IGBT driver board is pin 3 of the 5-pin output connector. This signal is directly fed to the gate of the IGBT at pin 7.

D. CURRENT AND VOLTAGE SENSOR CIRCUITS

To obtain the required inputs to the control circuit in Figure (4-1), current and voltage measurements had to be obtained from the power section of the SSCM.

1. Current Sensor Circuit

To obtain the $i_o/5$ and $i_L/5$ inputs to the control card, the circuit in Figure (4-7) was utilized (note, detailed schematics are included in Chapter V).

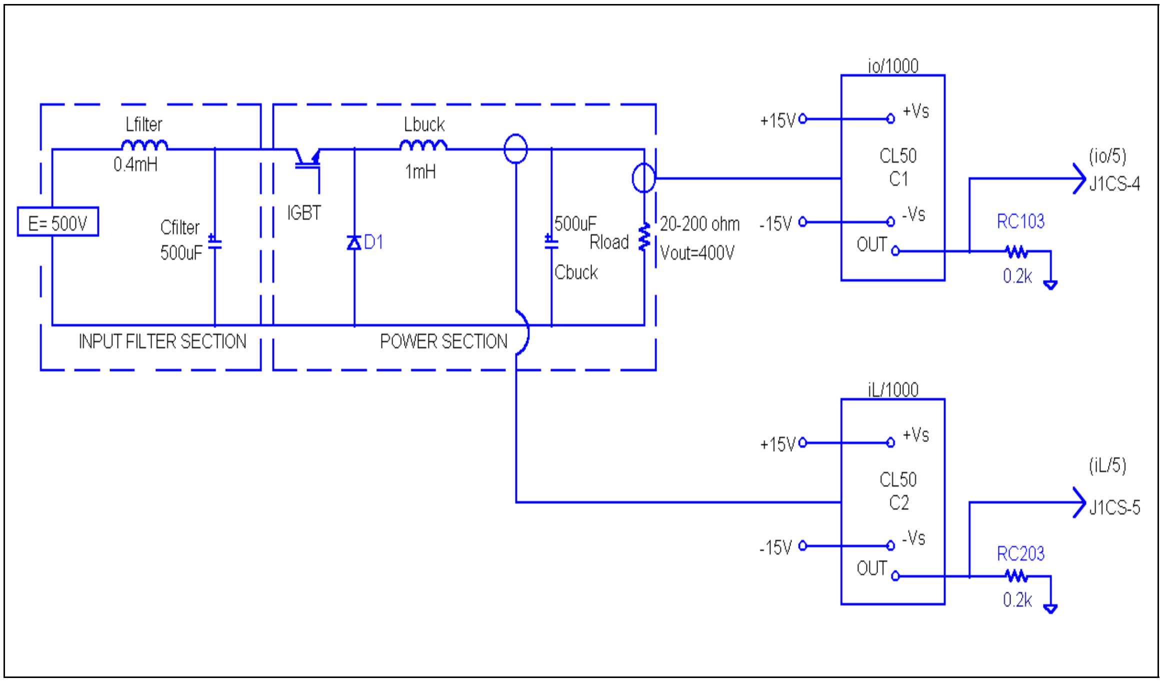


Figure 4-7, Current Sensor Circuit.

The theory of the CL50 Hall-effect sensor was described in Chapter III. From Figure (4-7), the CL50 requires a ± 15V supply (discussed in Chapter V). Chapter III stated that the CL50 divides whatever current flows through the device by 1000. With this in mind, average full-load current anticipated to be produced by the CL50 would be $\frac{20\text{A}}{1000} = 0.02\text{A}$. Next, given a 200Ω resistor, a 4V signal ($i_o/5$ and $i_L/5$) is achieved. The maximum output voltage of the sensor is 8V corresponding to a peak converter current of

40A. This leaves sufficient headroom for dynamic current measurements during transients.

2. Voltage Sensor Circuit

To obtain the required voltage inputs to the control circuit in Figure (4-1), voltage measurements also had to be readily available from the power section of the SSCM. Figure (4-8) illustrates where the measurements were obtained.

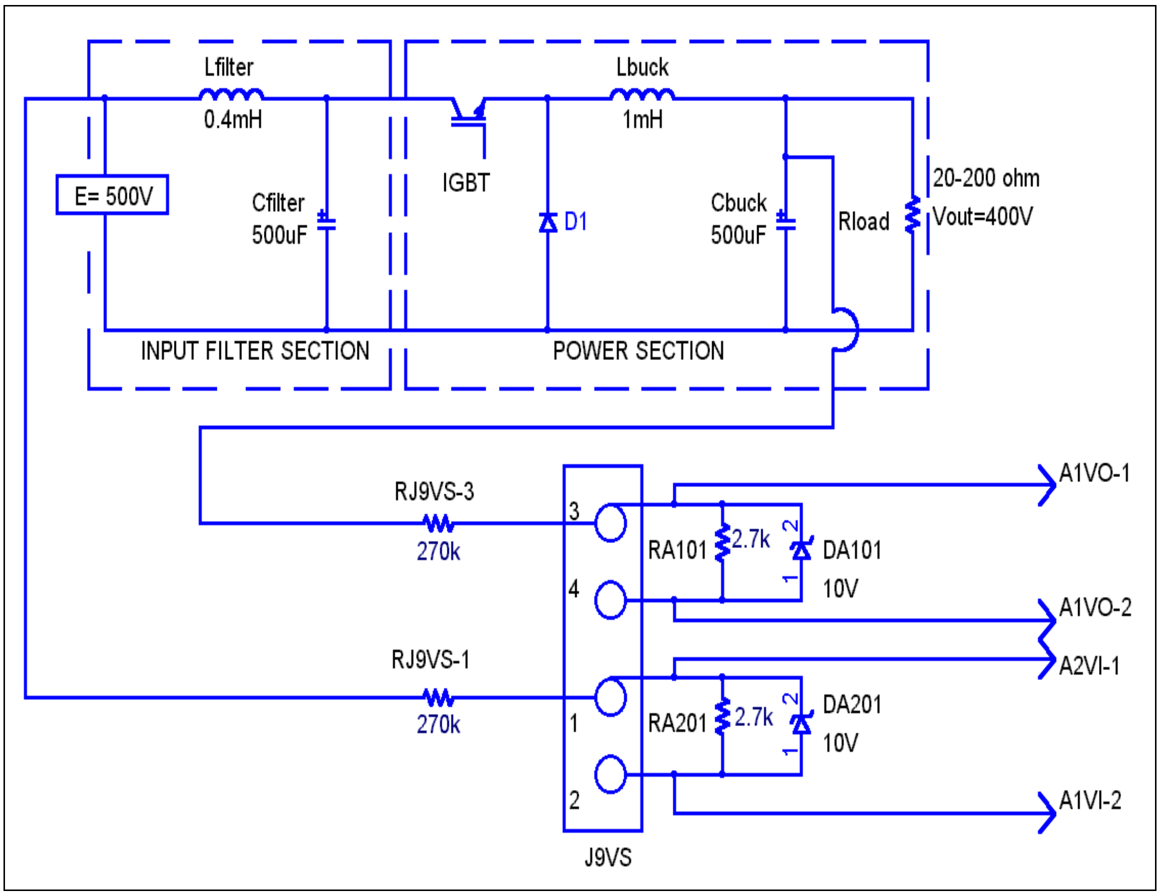


Figure 4-8, Voltage Sensor Circuit.

As shown in Figure (4-8), V_{in} (E) and V_{out} are taken from the input filter section and power section, respectively. Both signals are immediately sent through voltage divider networks consisting of 270kΩ and 2.7kΩ resistors. The zener diodes (DA101 and

DA201) prevent excessive voltages from entering the main control board. Equation (4-16) provides an example of the output to A1 (AD215 located on the main circuit board). Assuming V_{out} = 400V:

$$V_{A1V1} = V_{out} \times \frac{2.7k\Omega}{2.7k\Omega + 270k\Omega} \approx 4V \tag{4-16}$$

This simple circuit takes the high voltage from the power section and provides a much lower voltage to be used in the control circuitry of Figure (4-1). Circuit interface will be discussed in Chapter V.

E. SUMMARY

This chapter focused on the development of the control circuit for the SSCM. Also introduced were the sensor circuits that provide the required inputs for the control circuit, Figure (4-1). Stability verification was obtained using MATLAB, and proof of stability was illustrated via Bode plots. In Chapter V, circuit-labeling schemes are presented. Furthermore, detailed explanations of the protection circuitry, power supply and buffer stage are discussed. Also presented in the next chapter are the detailed schematics of all the sub-circuits. Placement of all schematics in Chapter V will allow the user to reference one chapter for all circuits in the SSCM.

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V. OVERALL CIRCUIT LAYOUT AND SCHEMATICS

A. PURPOSE

The purpose of this chapter is to unify the concepts introduced in Chapters II-IV. Schematics of the final product are illustrated and a functional description of each circuit and how they interconnect is presented. Circuit/schematic labeling is explained and problems (if encountered) in the assembly of the dc-dc converter are addressed. Appendix C contains a component parts list of each major sub-assembly discussed. The purpose of the parts list is to provide a ready reference to assist in the construction of additional units in the future.

B. CIRCUIT BOARD BACKGROUND

1. Board Cutting

Circuit board development was accomplished using Protel Easytrax software, version 2.06. Easytrax allowed layout and component interconnection on two layers (front and back). The software and necessary hardware were available at the Naval Postgraduate School. ET3 Yenko, lab assistant, manufactured all printed circuit boards for the SSCM.

All circuit boards were cut so that there were two separate ground planes: one isolated ground section for high voltage and a control card ground plane. Thermal pads were added at all connection points on the ground planes for ease of soldering. A thermal pad is a star cut around a hole in the copper made to reduce heat flow during soldering. Due to physical cabinet size limitations and desired circuit board location, the board was designed to ensure that all components would fit on a 10.75-inch by 6-inch board. This proved to be challenging since one goal was to limit the amount of "vias" on the board. A "via" is simply a jumper through which a signal on one side of the board is made available on the other side of the board. Trace widths were chosen based on perceived

current flow; thus power supply traces are significantly wider than signal traces. Connectors were placed strategically near the board edge to ensure ease of user access. Additionally, enough real estate was made available to accommodate heat sinks for the linear voltage regulators, LM 7815 and LM 7915.

Once a printed circuit board was developed, a netlist was compiled. The netlist associates integrated circuits with resistors, capacitors, and diodes allowing connections to be verified. Netlists and component lists are provided in Appendix D. Once a printed circuit board was completed, a Gerber file was generated. The purpose of the Gerber file is to direct the milling machine to drill at the required locations for component placement on the circuit board. Circuit layout printouts from Easytrax are provided in Appendix D.

2. Circuit and Schematic Labeling Schemes

To ensure ease in locating components and to understand their function in the circuit, a labeling system was developed. The first symbol represents the physical component, for example:

- C: capacitor,
- A: AD215 voltage isolators (A1-A2),
- D: diode,
- R: resistor,
- S: switch (S1),
- U: IC chip (U1-U9),
- J: connector or BNC connection (J1-J10),
- Q: transistor (Q1-Q3).

The second digit represents what IC the component is associated with, for example:

- R3: resistor associated with IC #3,
- C1: capacitor associated with IC #1.

The third and fourth digit tell what pin number the component is connected to, for example:

- R109: resistor associated with IC #1 pin 9,

- C210: capacitor associated with IC #2 pin 10.

If multiple components of the same type are connected to the same pin of an IC, a letter suffix is added. For example, R102A, R102B, and R102C are three separate resistors connected to IC #1 pin 2.

Other suffixes used are listed below:

- G: ground,
- Q: transistor,
- H: VCC high,
- L: VCC low,
- Z: identifies a jumper.

A few final examples of circuit labeling are offered:

- R603H: resistor associated with U6 pin 3 and VCC high,
- J9VS: connector J9 from voltage sensors,
- J1CS: connector J1 from current sensors,
- J2FP: connector J2 from front panel.

C. CIRCUIT DIAGRAMS AND DESCRIPTIONS

This section documents the hardware implementation of the buck converter as well as the associated sensor and control circuits, and driver board. Each subsection is organized so that it contains a detailed schematic and description of the circuit. If further detail is desired, Appendix D contains the Easytrax schematics and the netlists.

1. SSCM Buck Converter Topology

Figures (5-1) and (5-2) illustrate the layout for the buck converter input filter, power section, and circuit feeds to the voltage and current sensing circuits. Components for the input filter and power section were discussed in Chapter III. The following provides the general flow for the overall system:

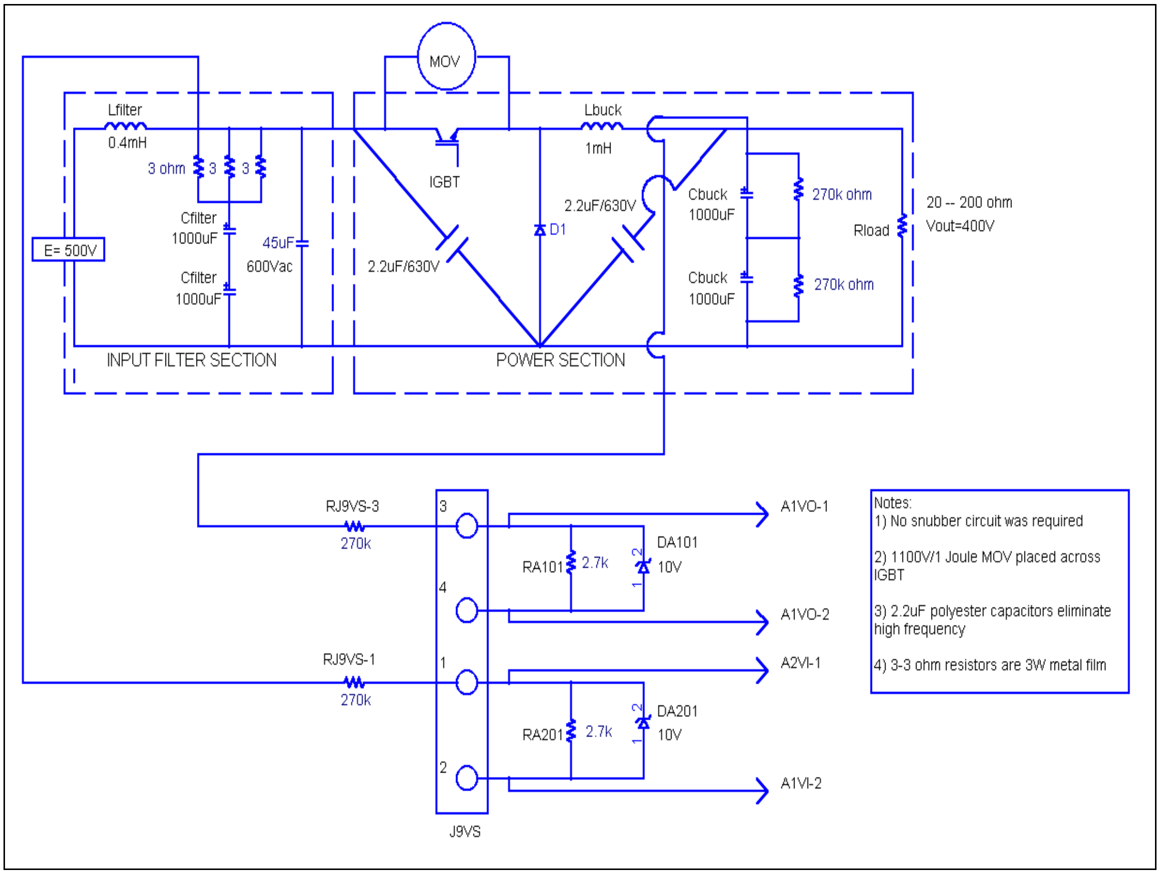


Figure 5-1, Buck Converter Voltage Sensing.

- 500VDC input power source is applied to the range plug located on the rear panel of the SSCM. This is depicted as the block containing (E = 500V) in the schematic above.
- In Figure (5-1), sensed voltages from the voltage divider networks are sent via twisted pair to J9VS (located on the main circuit board). Through this voltage divider network, $V_{in}/100$ and $V_{out}/100$, via a buffering circuit, are made available to the control circuitry.
- As illustrated in Figure (5-2), sensed currents are sent to the main control board via Hall-effect sensors located underneath and aft of the main circuit board. A 200Ω resistor (located on the Hall-effect sensor board) provides the necessary scaling factor to achieve $I_L/5$ and $I_{out}/5$, which are then made available to the control circuitry via the buffering circuitry. Scaled currents

enter the main control board through connector J1CS (illustrated in a later section).

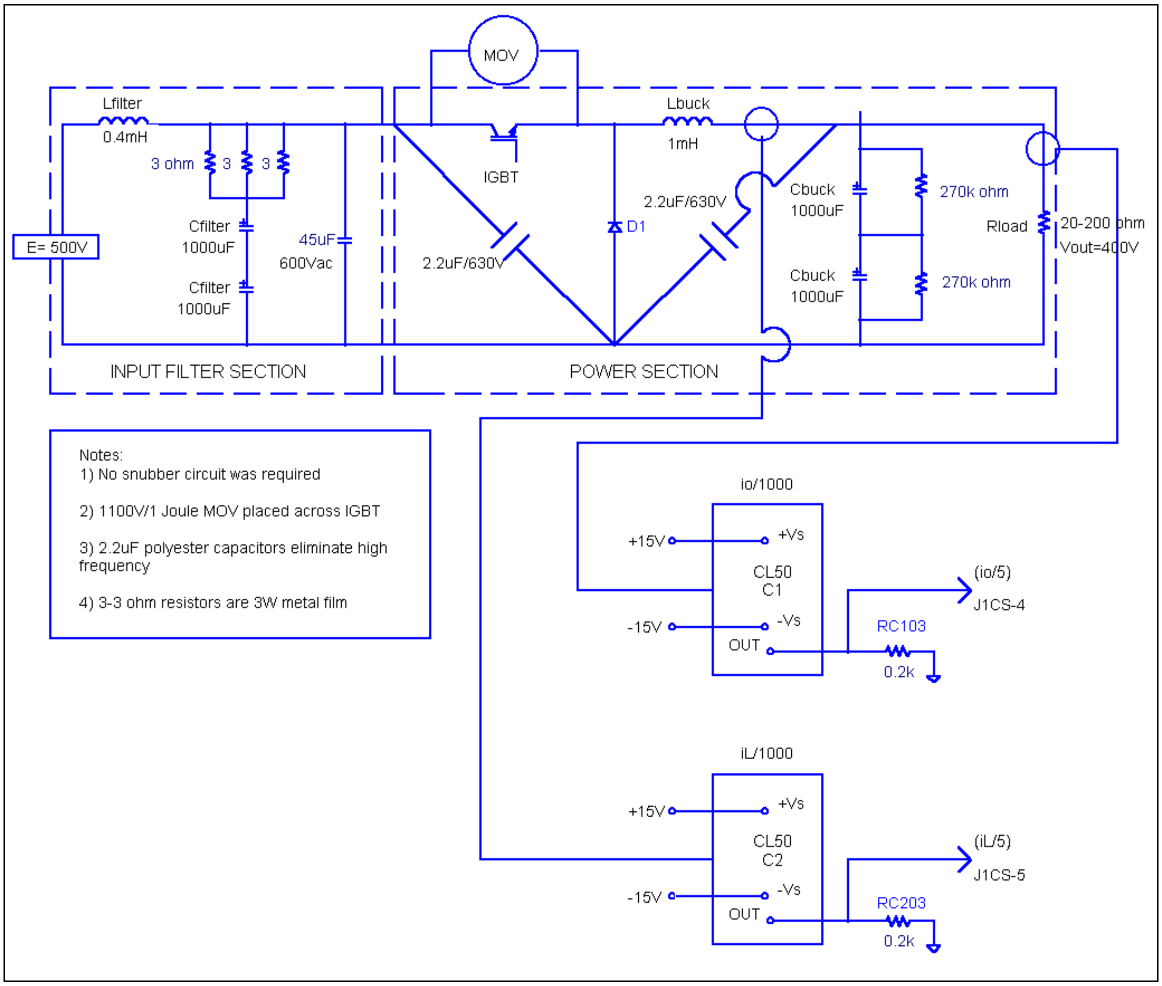


Figure 5-2, Buck Converter Current Sensing.

- The control circuitry processes the voltages and currents according to the developed control algorithm outlined in Chapter IV.
- The generated driver signal from the control board is sent to the PWM circuitry. The PWM signal is sent to the IGBT driver board to gate the IGBT.

With this general flow of events outlined, a more detailed description is presented.

2. Sensor Boards

Pictured in Figures (5-3) and (5-4), the sensor circuits/boards provide isolation between the buck chopper power section and the control board. Sensed voltages from the voltage divider network on the buck converter are sent via twisted pair wires to the input of the wideband AD215 isolation units. Configured as unity gain buffers, the AD215s output the sensed voltages and send them to the buffer stage located on the main circuit board.

Current sensing is achieved by the use of the CL50 mounted on its own circuit board underneath the main circuit board (Figure (5-4)). Instantaneous currents proportional to (i_{sensed}/1000) are output by the Hall sensors. These currents are immediately converted to proportional voltages by 200Ω resistors located on the current sensing board next to the CL50. The signals obtained, (i_{sensed}/5), are sent to J1CS pins four and five via ribbon cable.

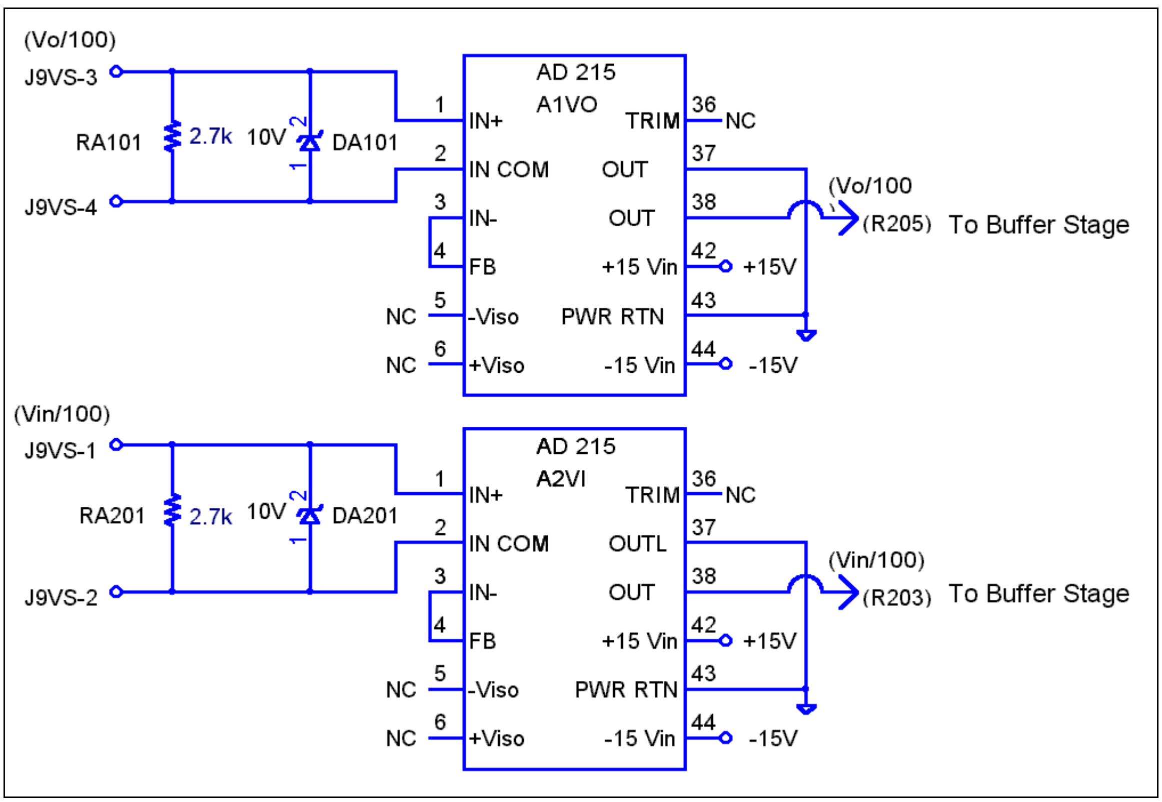


Figure 5-3, Voltage-Sensing Circuit.

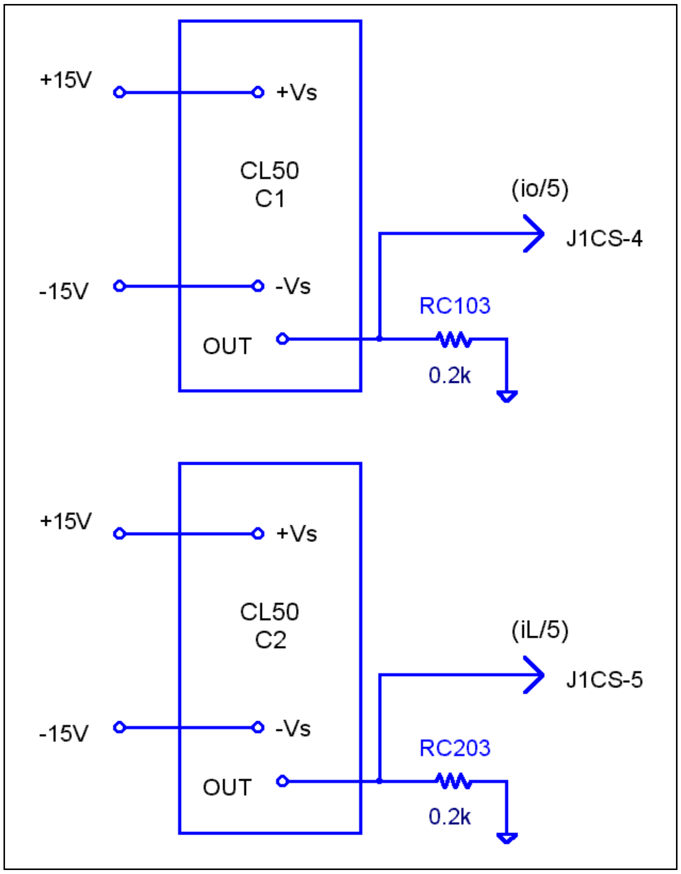


Figure 5-4, Current-Sensing Circuit.

3. Main Circuit Board

The main circuit board can be broken down into five subsections:

- Power supply stage,
- Buffer stage,
- Main control stage,
- Pulse width modulation stage,
- Protection circuitry stage.

A schematic and discussion of each of the subsections follows.

a. Power Supply Stage

Illustrated in Figure (5-5), the power supply receives $\approx 117V_{AC}$, 60Hz receptacle power through a 36Vct/1A step-down transformer. The thirty-six volt transformer output enters the main circuit board through J10AC where the voltage is rectified to produce $(\pm)$ $28.2V_{DC}$ (measured). The voltage is then sent into voltage regulators U8P (+15V) and U9N (-15V).

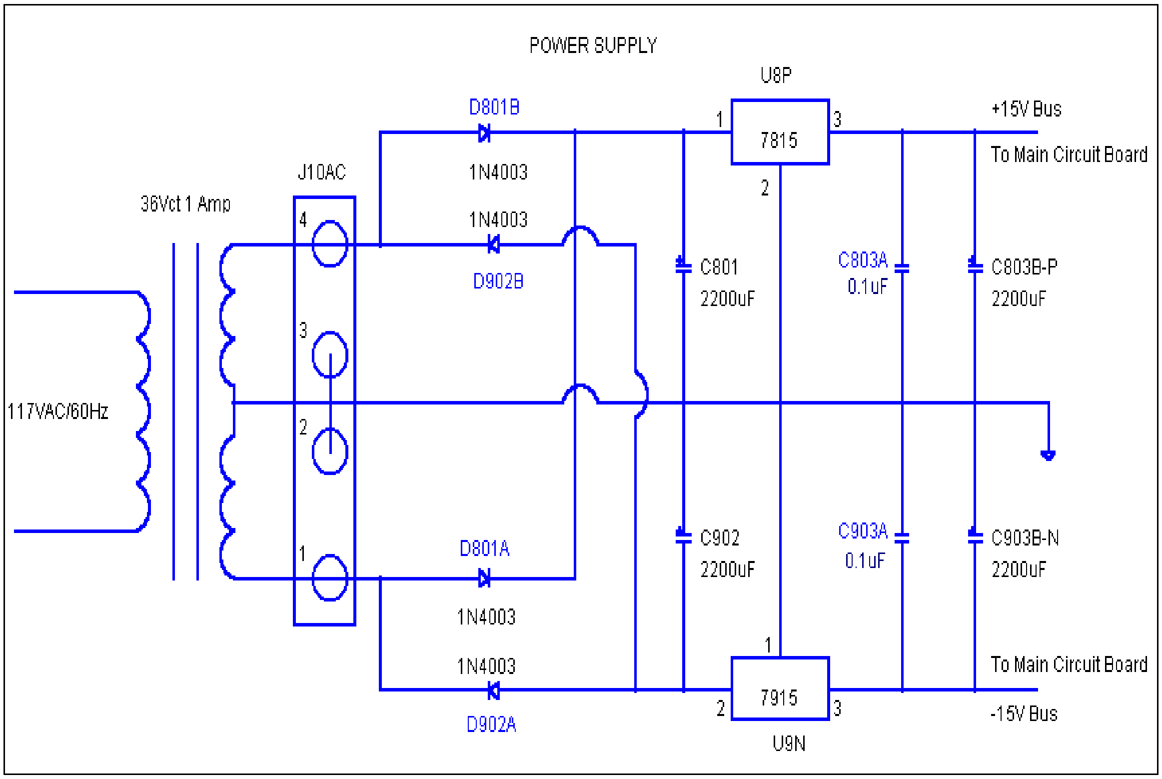


Figure 5-5, Main Circuit Board Power Supply.

From the voltage regulators, $(\pm)\,15V_{DC}$ is distributed via busses located on the main circuit board. This voltage is used to power all of the integrated circuits on the main circuit board. Actual output values were:

- U8P pin three positive voltage = $15.19V_{DC}$,
- U9N pin three negative voltage = $15.20\ V_{DC}$.

b. Buffer Stage

As stated previously, the scaled currents and voltages enter the main circuit board through J1CS and J9VS, respectively. From J1CS and J9VS (and then through the AD215s), the inputs are buffered utilizing a LM324 quad op-amp (labeled U2) as illustrated in Figure (5-6). Each buffer stage input contains an RC lowpass filter designed to remove high-frequency components from the measured voltages and currents. Using Equation (5-1), the cutoff frequency for each filter is set at 20.095kHz (near the switching frequency of the IGBT). The frequency was initially set at 1.8kHz; however, during testing it was found not to be required since the input to the PWM chip possesses a 1.8kHz filter. The LM324 outputs are fed to the main control stage.

$$f_c = \frac{1}{2\pi RC} \tag{5-1}$$

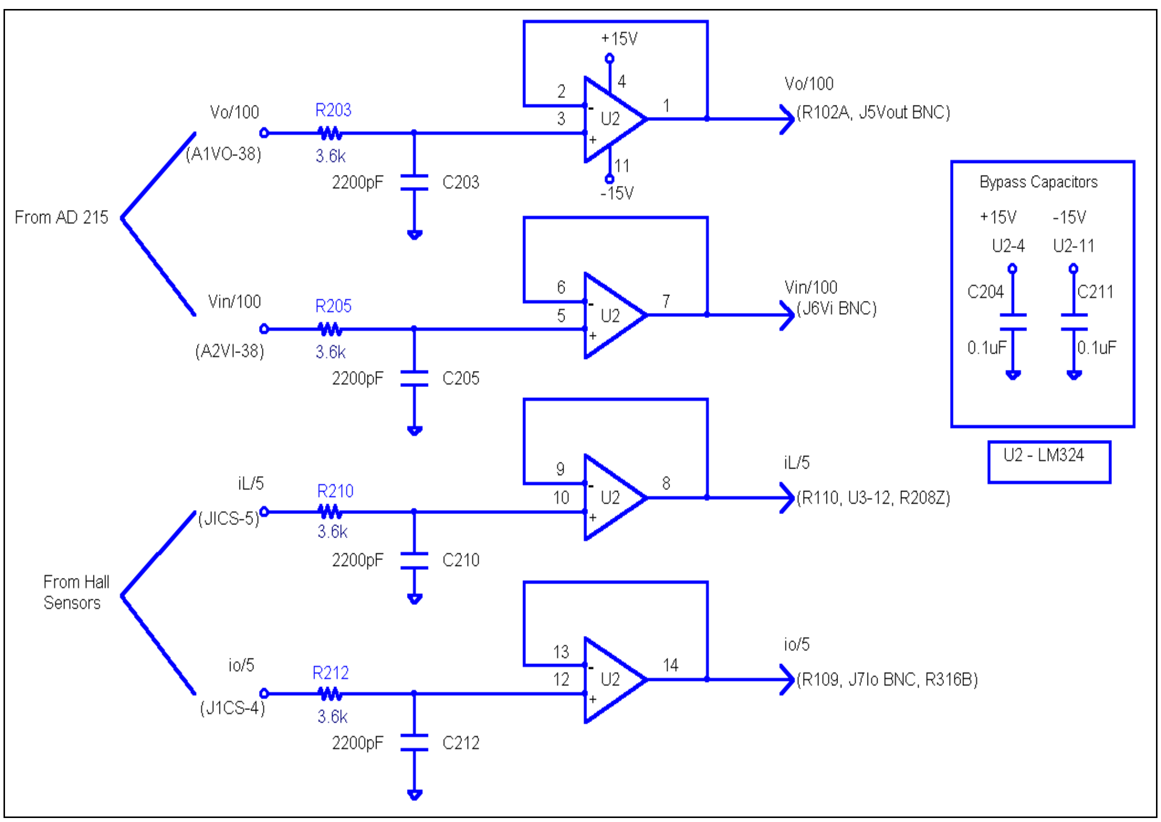


Figure 5-6, Buffer Stage.

c. *Main Control Stage*

The main control stage is where Equation (4-1) is implemented. The output of this stage is the duty cycle, d(t), scaled by a factor of ten. The main control stage was described in detail in Chapter IV and is illustrated in Figure (5-7). In addition to the buffer stage inputs, the signal representing the desired output voltage, $-V_{ref}/100$, is fed into the main control stage from the protection and startup circuitry stage.

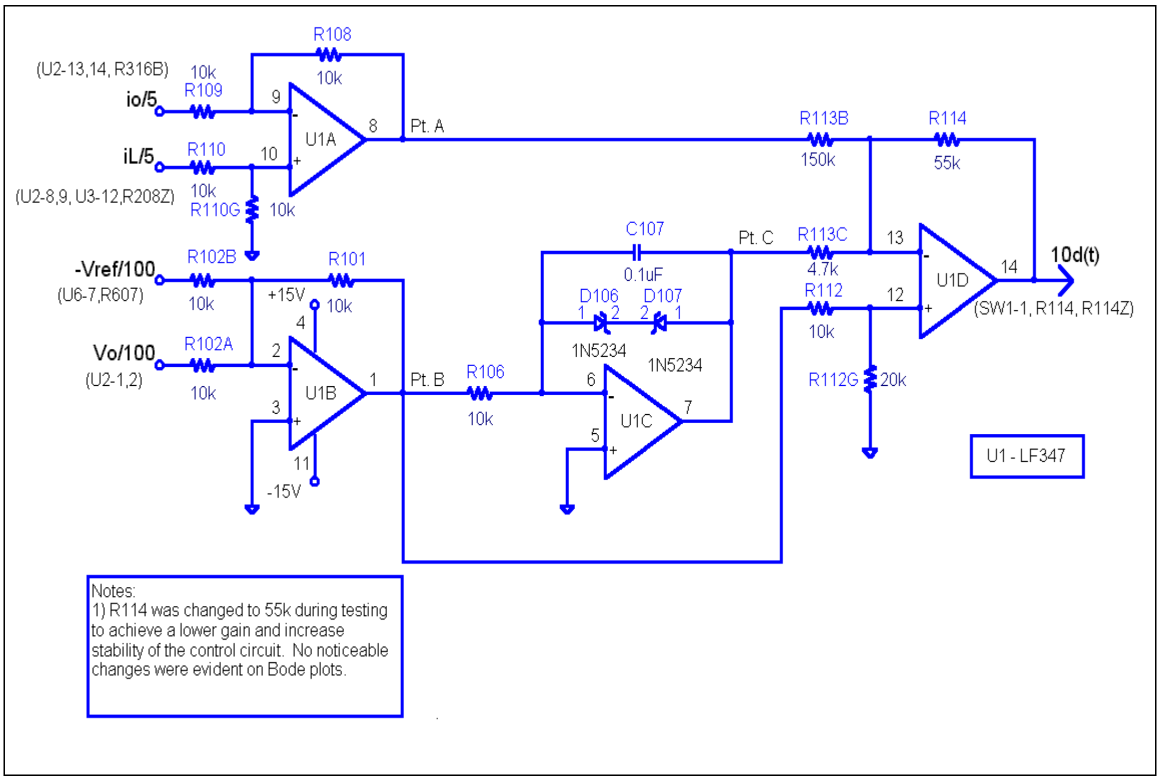


Figure 5-7, Main Control Stage.

The control algorithm is performed using an LF347 quad op-amp. The first three op-amps in the package form the proportional voltage (U1B), integral voltage (U1C), and current response terms (U1A). Note that a limited integrator has been used to generate the integral voltage term. This configuration prevents integrator windup as previously defined in Chapter IV. Without the limiting zener diodes in place, C_{107} is free to charge up during extended transients to values well outside the range in which its voltage affects duty cycle. As a result, the voltage on C_{107} locks out the remaining terms

in the duty cycle control algorithm. This lockout persists until C_{107} comes back within its operating range. The final op-amp, U1D, is used to scale and sum the outputs of the first three op-amps. The output of the main control stage feeds the user select switch, SW1 (eight position dip switch), located on top of the main circuit board. When this switch is positioned with one and two in the "on" position, the signal is fed to the pulse width modulation stage. In Figure (5-8), the user select switch is illustrated. The schematic details all SW1 switch positions. The closed position in the schematic is equivalent to "on" in the table. The user select switch allows the operator to either utilize the controller inside the SSCM or to simply use an externally generated duty cycle. In the latter case, SW1-2,3 (switch 1, position 2 and 3 "on") would be placed in the "on" position and the BNC labeled J4DR would be interfaced with the desired external duty cycle signal.

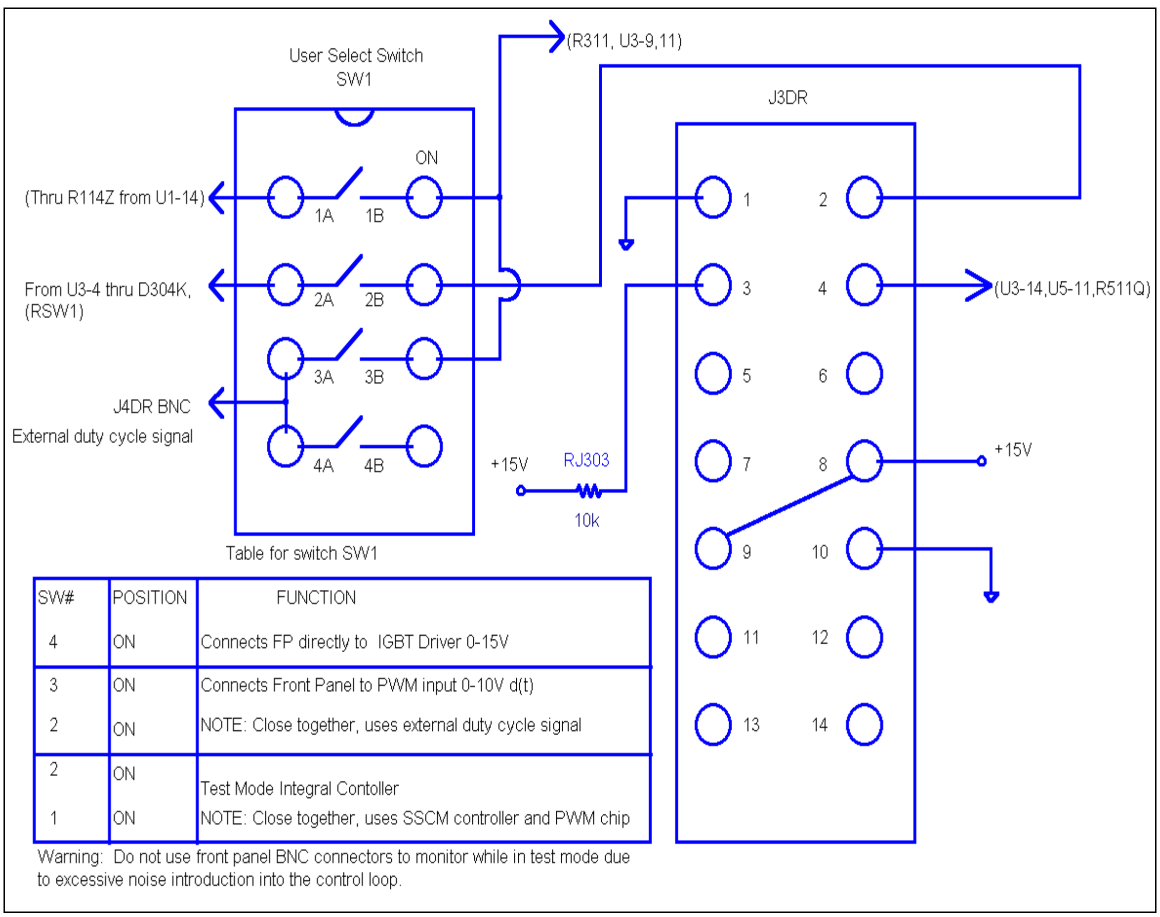


Figure 5-8, User Select Switch.

d. Pulse Width Modulation Stage

Illustrated in Figure (5-9) is the pulse width modulation (PWM) stage. The PWM stage is comprised of the UC3637 chip. When the user select switch is positioned so that one and two are in the "on" position, the duty cycle from the main control stage is received. The function of this stage is to produce a 20 kHz PWM signal (0-15V) to feed the IGBT driver board that in turn gates the IGBT as per the specifications dictated by ESAC. Frequency was determined by calculating the required values of R_{318} and C_{302} as described in the UC3637 data sheets. Chapter III detailed the process. The actual measured frequency is 20.38kHz.

R_{311} and C_{311} were selected to provide approximately one-decade frequency separation between the input signal and the IGBT switching frequency (f_{cutoff} = 1.88kHz). D_{311} functioned to limit the input to ten volts. The duty cycle represents a signal between zero and 100 percent or equivalently zero to ten volts. For example, eight volts equals 80 percent duty cycle. D_{311} therefore functions to maintain the duty cycle below 100% ($\approx$95%). This wanted limitation avoids the possibility of a narrow pulse near 100% duty cycle, which in turn prevents the IGBT from turning on. R_{313} and C_{313} are part of the protection circuitry and will be described in the next section. D_{301} sets the upper threshold voltage at 10V as described in Chapter III (Equations (3-14) and (3-15)). Detailed specification sheets for the UC3637 are located in Appendix A.

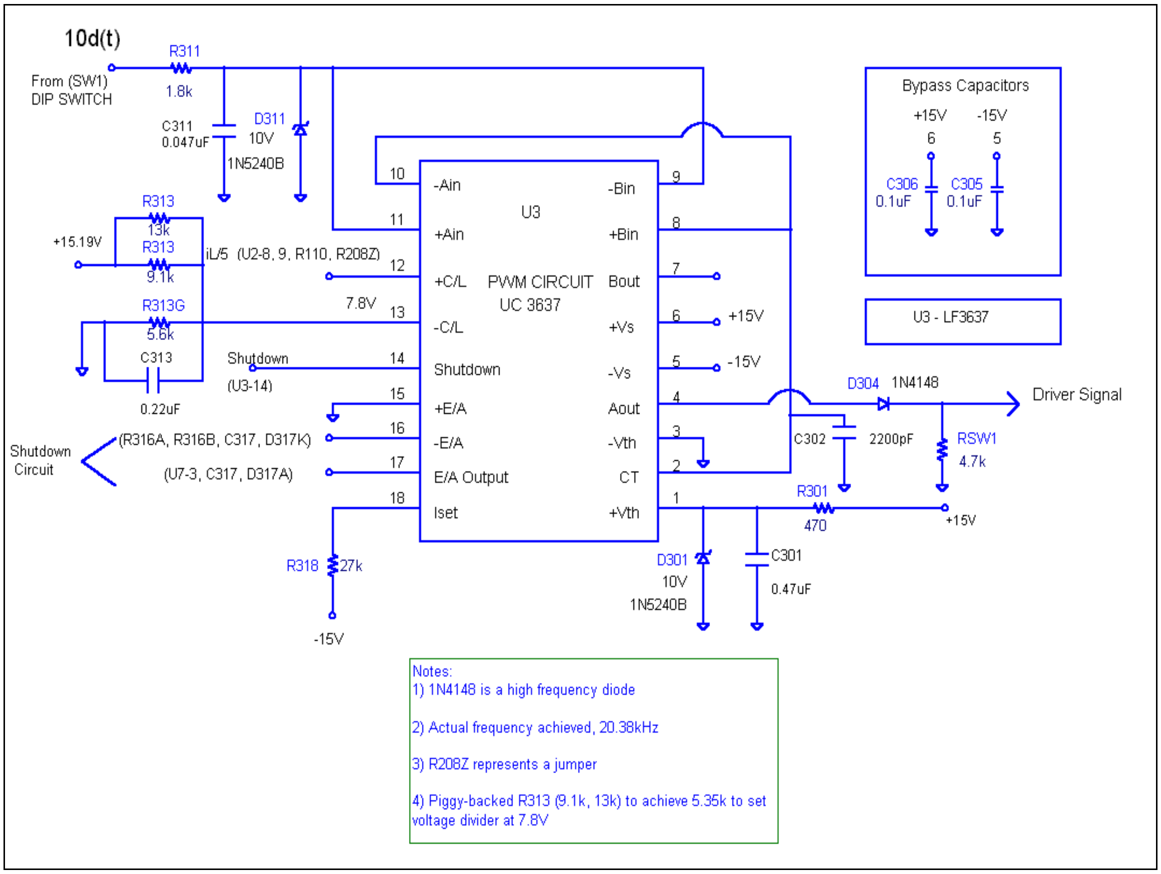


Figure 5-9, Pulse Width Modulation Stage.

e. Protection Circuitry Stage

The analog controller provides the buck chopper with two forms of protection. The first is the pulse-by-pulse current limiting feature of the UC3637 chip. This simple circuit protects the Semikron IGBT from exceeding its 100A current rating. Referring to Figure (5-9), pins 12 and 13 comprise this circuit. The voltage signal from the current sensor board, $i_L/5$, is applied to pin 12. If a fault occurs at the output of the dc-dc converter, $i_L/5$ will increase. The voltage at pin 13 is fixed by the voltage divider network consisting of the piggyback resistors R_{313} and R_{313G} and the +15.19V (measured) power supply. If its peak exceeds the voltage divider network, which is set at 7.8V (8V due to a 200mV built-in IC offset, see spec sheet in Appendix (A)), the IGBT driver signal coming from U3 pin four will go low. The PWM chip will evaluate the current at

the switching frequency. The IGBT will remain open until the peak inductor current falls below this overload threshold value.

The second protection circuit is over-current time-out. Part of this circuit is illustrated in Figure (5-10); the circuit in its entirety is shown in Figure (5-11). This circuit protects components from thermal damage when the output current exceeds $\approx$100% rated (20A) and is set to time-out in 300msec at $\approx$125% rated current (25A). A description of the circuit operation and design is presented next.

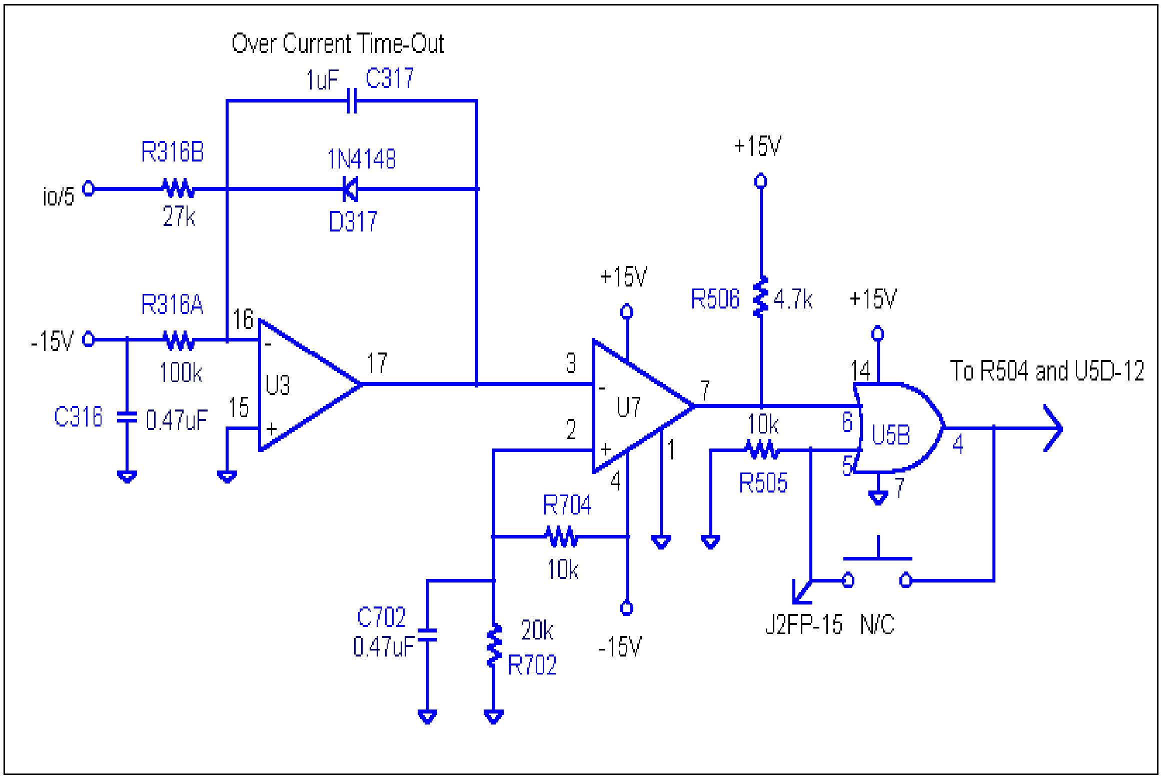


Figure 5-10, Over-Current Time-Out Timing Circuit.

D_{317} prevents the integrator from operating until $\dfrac{i_o/5}{27k\Omega} > \dfrac{15.2V}{100k\Omega}$ (using the actual negative supply voltage of -15.2V) or (i_o > 20.52A). Thus R_{316A} and R_{316B} establish the set point for the beginning of integrator operation. Once i_o exceeds 20.52A (found to be 21.82A experimentally), C_{317} begins to charge linearly based on a constant overload current.

The comparator circuit consisting of U7, R_{704}, and R_{702} establishes the trip voltage of the integrator at -10.133V (using the actual negative supply voltage of -15.2V). If a constant 125% overload current is assumed, then the time to trip the circuit may be determined as follows. Given that $I = C\frac{\Delta V}{\Delta t}$ where C = 1μF, ΔV = 10.133V, and I = (25A-20.52A)/(5*27kΩ) = 331.185μA (using I_o = 25A), Δt = 305msec. Note, this can be placed in one equation and solved using Equation (5-2) where V_{out} refers to the output of U3.

$$V_{out} = -\int_0^t \left(\frac{1}{R_{316B}C_{317}}(i_o/5) + \frac{1}{R_{316A}C_{317}}(-15.2V) \right) dt + v_{out}(t=0) \qquad (5\text{-}2)$$

Choosing to solve for the time, all values from Figure (5-10) are directly substituted into Equation (5-2) and the expression is integrated from 0 to t. The initial value of $v_{out}(t)$ is zero and the final value is -10.133V. After substitution, Equation (5-2) reduces to Equation (5-3).

$$-10.133V = -185.185t + 152t \qquad (5\text{-}3)$$

Solving for the trip time yields $t \approx 305$msec. A similar analysis can be performed for additional values of continuous overload current. Results are summarized in Table (5-1).

$\mathbf{I_o}$	**Δt**
21A	2.851 sec
22A	0.924 sec
23A	0.552 sec
24A	0.393 sec
30A	0.144 sec

Table 5-1, Theoretical Over-load Circuit Trip Times.

As just described, the op-amp in U3 (pins 15-17) was designed such that $i_o/5$ = 5V causes pin 17 to reach -10.133V in approximately 300msec. This voltage trips comparator U7 high and causes U5B (latch) and U5D (fault summer, see Figure (5-11)) to go high. This signal is sent directly to U3 pin 14 initiating a shutdown at pin 14. This shutdown signal immediately disables the driver signal at pin 4 of U3, stopping buck chopper operation.

The startup circuitry depicted in Figure (5-11) allows the duty cycle to ramp up to its steady-state value from zero initial conditions. When the controller is initially energized, U5A goes high due to a +15V pulse generated by the RC circuit at pin 1 of OR gate U5A (RC circuit is made up of C_{501} and R_{501}). As a result, U5D goes high turning on Q1 (and disables the PWM chip). With Q1 "on", capacitor C_{603} is effectively "shorted" making pin 3 of U6A $\approx$ 0V preventing a reference signal from being generated. This action prevents a high duty cycle waveform from being generated during start-up, which, could result in large current and voltage oscillations possibly damaging the converter. By resetting the over temperature push button on the front panel, Q1 is turned "off" and the reference voltage is allowed to "ramp-up". Reference voltage is controlled from the front panel by adjusting the potentiometer and monitoring the front panel digital meter. The reference voltage ramps up to its final set point through the action of the RC time constant set by R_{603} and C_{603} (τ = 1 sec). U5C was not utilized in the design and was therefore grounded to prevent possible interference.

Over-temperature control was achieved by the use of a thermistor switch (see Appendix C), which is located directly above the IGBT (on the same heat sink). When the temperature exceeds 157 degrees Fahrenheit (70°C), the thermal switch pulls pin 1 of U5A high through J1CS-1. This causes a shutdown and lights the TEMP LED on the front panel to warn the operator. Note, once the temperature has decreased below 157 degrees, the user must reset the LED by depressing the over temperature pushbutton on the front panel (see Figure (2-2), front panel). Thermistor selection was based on the upper temperature parameter of the IGBT (85°C).

Both over-current time-out and thermal overload can be reset using the front panel. However, if the protection circuitry in the "smart" IGBT driver board is

activated due to a fault condition, all input power must be removed from the converter and the control power must be cycled off and on to reset the card (no LED indication for this fault). This condition was inadvertently tested at full voltage by mistakenly switching from a 25% load condition to a short-circuit load during transient testing. The converter survived the ordeal, but the external transient load switch was destroyed.

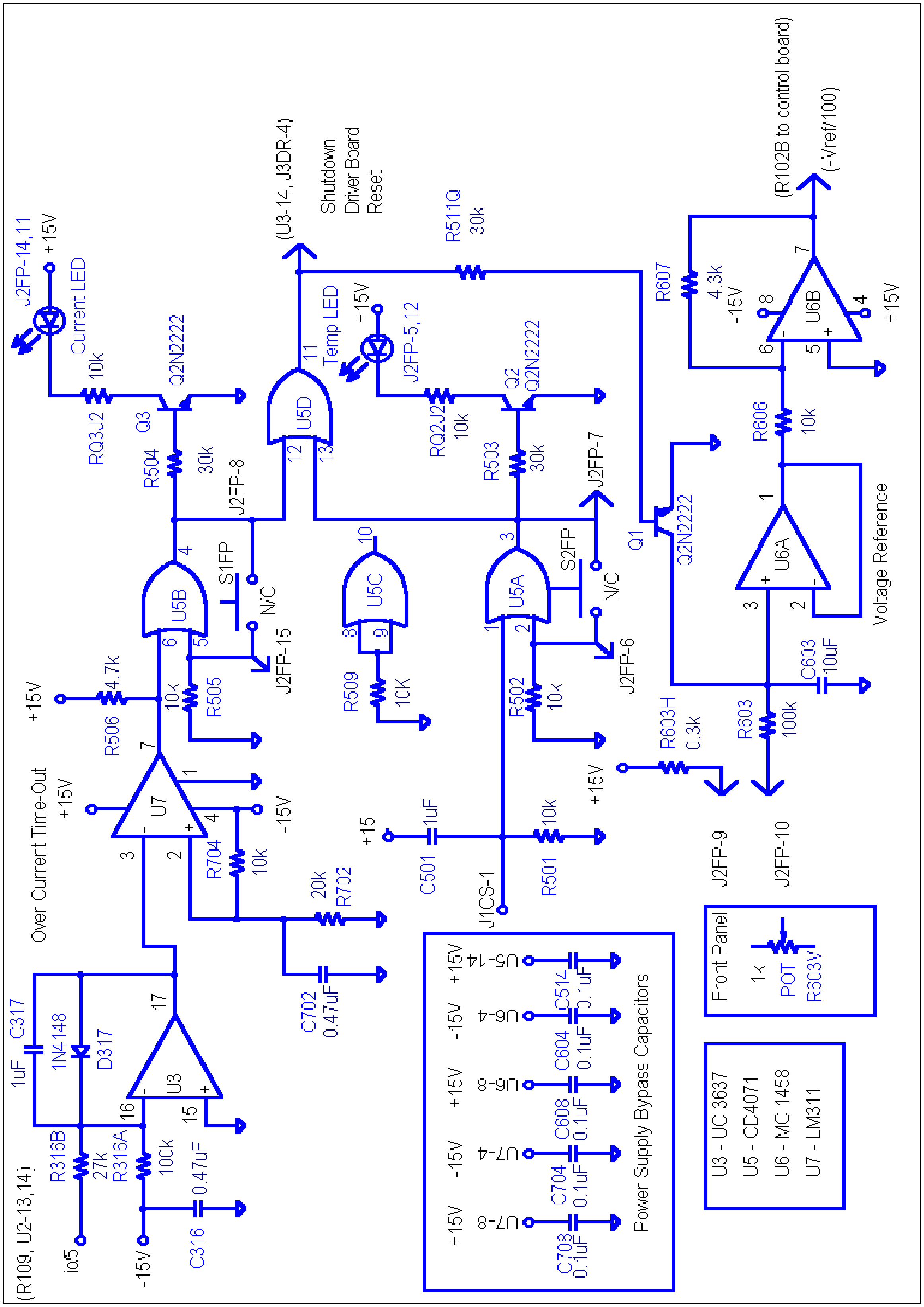


Figure 5-11, Protection and Startup Circuitry Stage.

4. IGBT Driver Board

As previously discussed, the IGBT driver board utilized in this design was Commercial-Off-The-Shelf (COTS) Technology from SEMIKRON. Detailed schematics and circuit operation are described in Appendix A. The only modification to the driver board was to bridge the solder gap (J2). When only one IGBT is to be gated, this is a recommended procedure.

The output of U3-4, the gating signal, goes through fast recovery diode D_{304} directly to the IGBT driver card through J3DR-2 (see Figures (5-9) and (5-13)). D_{304} functions to pass only the positive portion of the signal leaving U3-4. This signal is fed to the 14-pin connector pin 2 on the IGBT driver board. The output of the driver board exits the 5-pin connector at pin five which connects directly to the gate of the IGBT.

5. Miscellaneous Schematics

Figures (5-12) through (5-15) illustrate the wiring for all connectors utilized in the design process. Figure (5-12) pictures the BNC connectors located on top of the main circuit board. These BNC connections were provided for operator convenience. Each main circuit card BNC is connected directly to the front panel of the SSCM in order to allow monitoring of system variables, see Figure (2-2).

In the four schematics that follow, circuit interfaces are written next to the applicable pin number on the BNC or the fourteen-pin connector. If connector pins are not used, the schematic will contain a note to indicate which pins. The only connector schematics absent in this section are the pin layouts for the IGBT driver board. Detailed schematics for the IGBT driver board and all its connectors are offered in Appendix A.

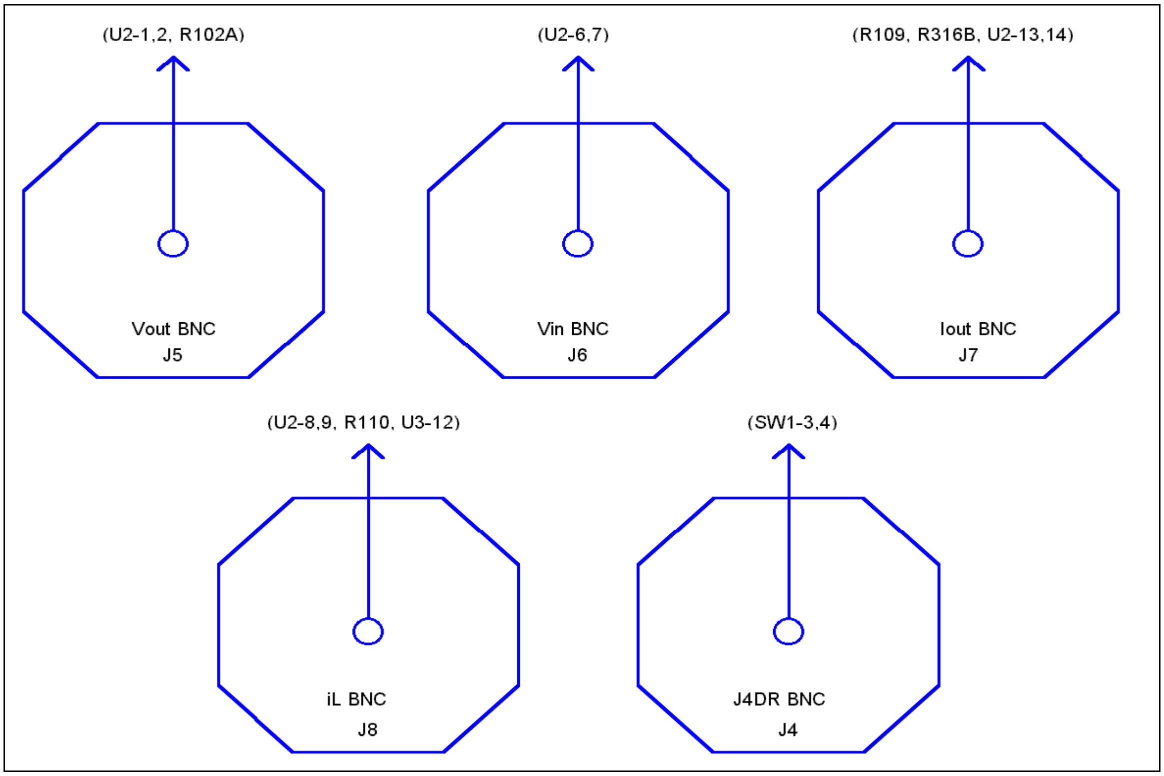


Figure 5-12, BNC Connectors on Main Circuit Board.

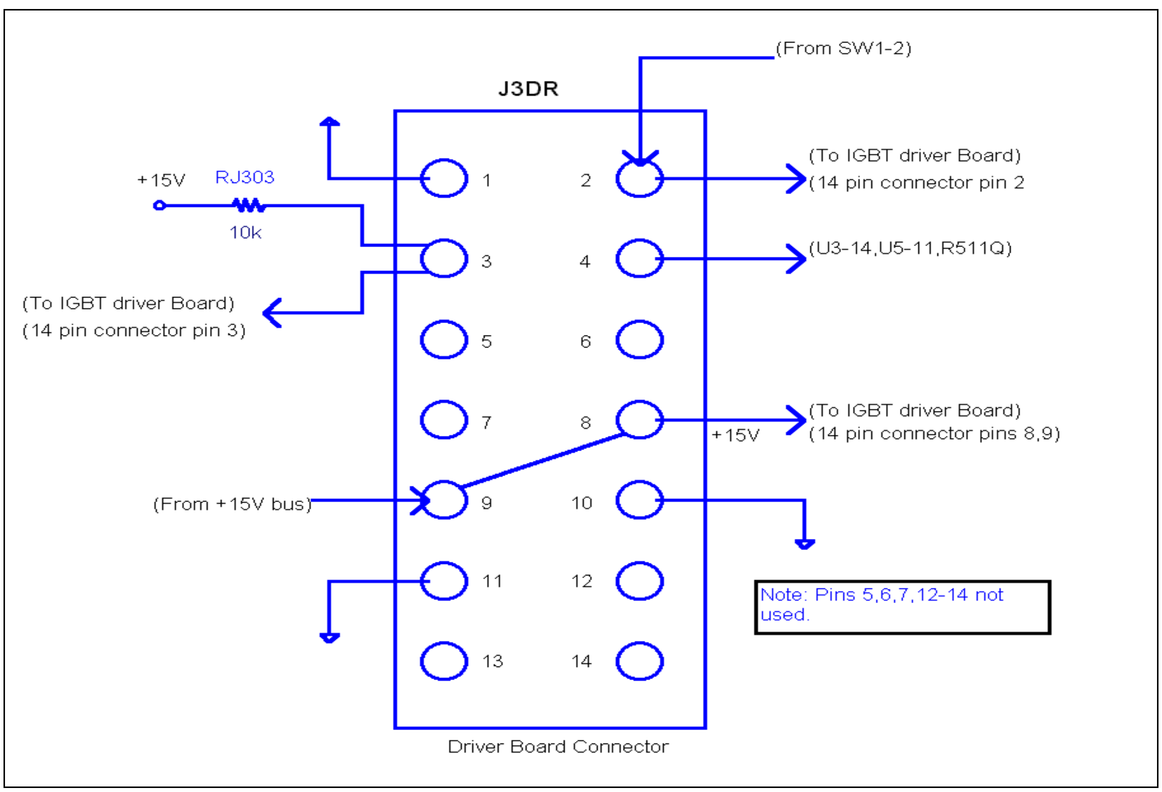


Figure 5-13, J3DR 14-Pin Connector on Main Circuit Board.

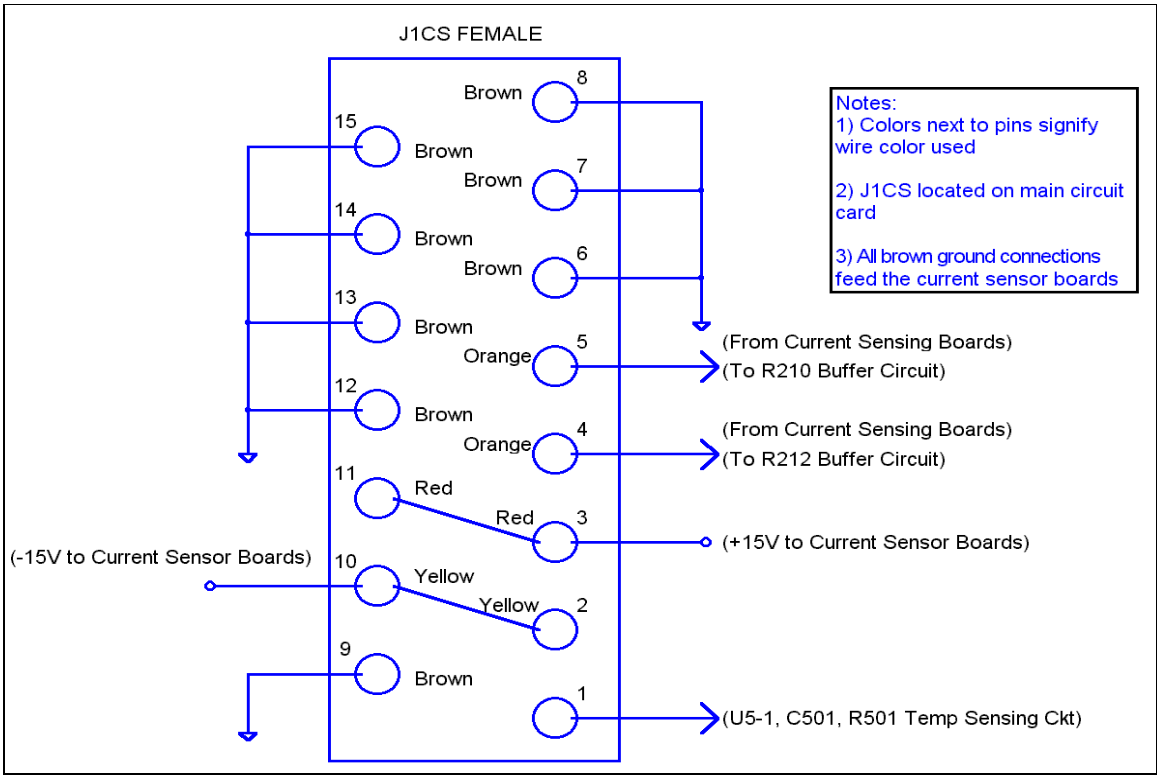


Figure 5-14, J1CS 14-Pin Connector on Main Circuit Board.

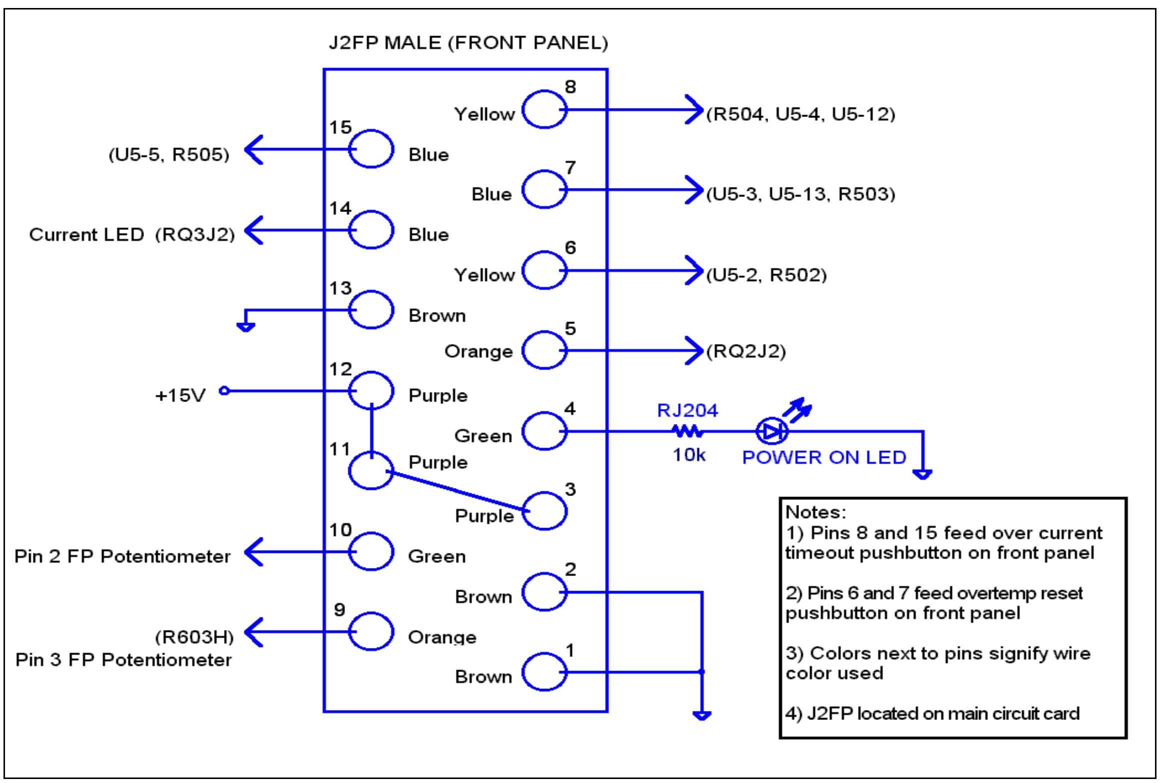


Figure 5-15, J2FP 14-Pin Connector on Main Circuit Board

D. PHYSICAL COMPONENT LAYOUT

The purpose of this section is to provide pictures of the SSCM during the assembly stages. Figure (5-16) depicts the assembled front and rear panels that were illustrated in Figures (2-2) and (2-4). The 3A fuse is for protection of the 115Vac input line while the 30A fuse protects the dc input line.

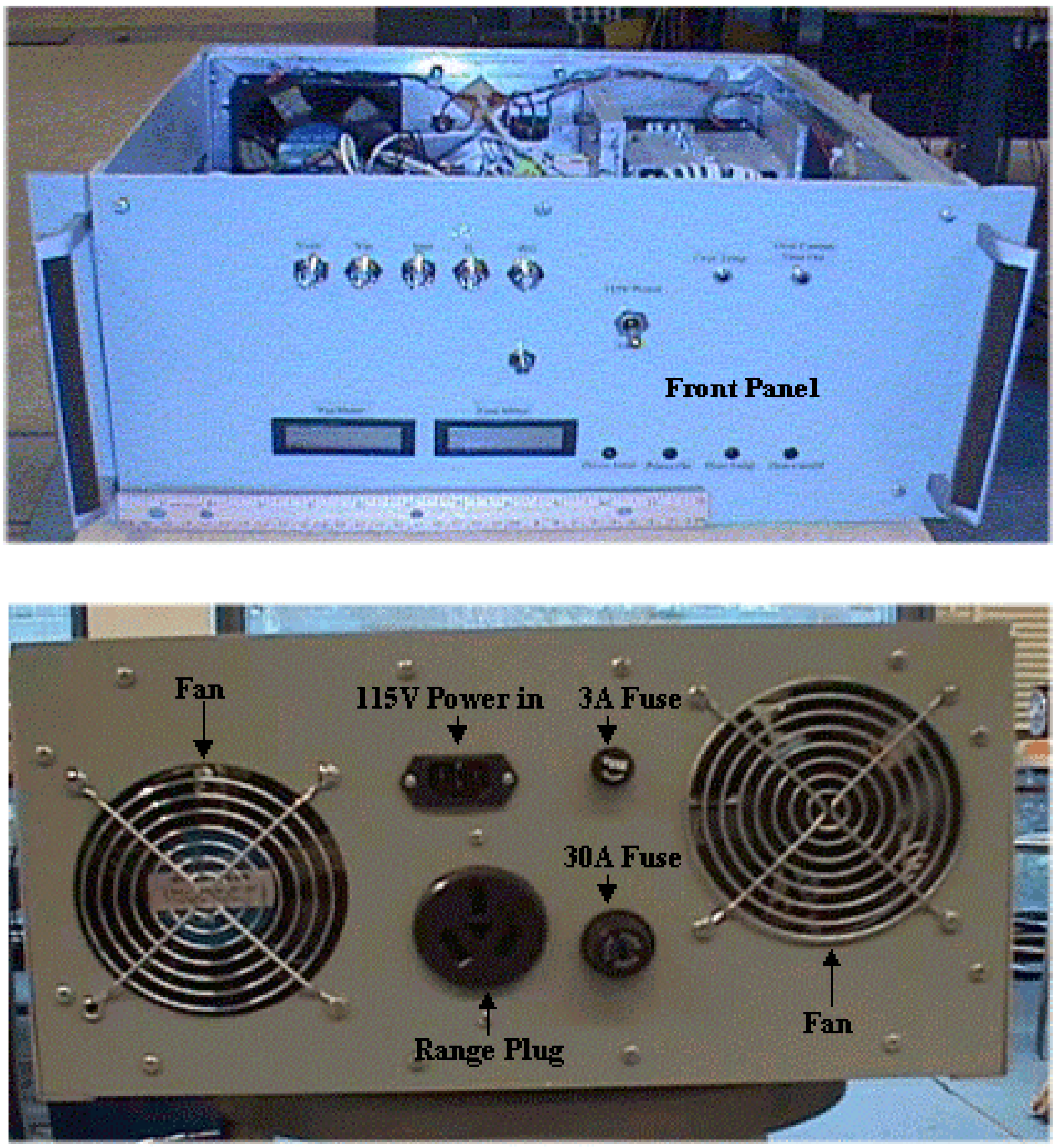


Figure 5-16, SSCM Front and Rear Panel.

In Figure (5-17), the placement of the heat sink, input filter, and power section is illustrated. To ensure maximum airflow across the heat sink fins, two fans were placed in the enclosure. The left-most fan pushes air into the unit while the right-most fan functions to force air across the fins and out the rear of the heat sink and unit. The high heat generating components were placed on or near the heat sink (IGBT attached to the heat sink side, power section inductor placed in front of heat sink). The input filter inductor produces minimal heat therefore its placement was not critical. An aluminum central support was installed to enhance ruggedness and provide support for the input and output capacitors and for the mounting of the current sensor boards.

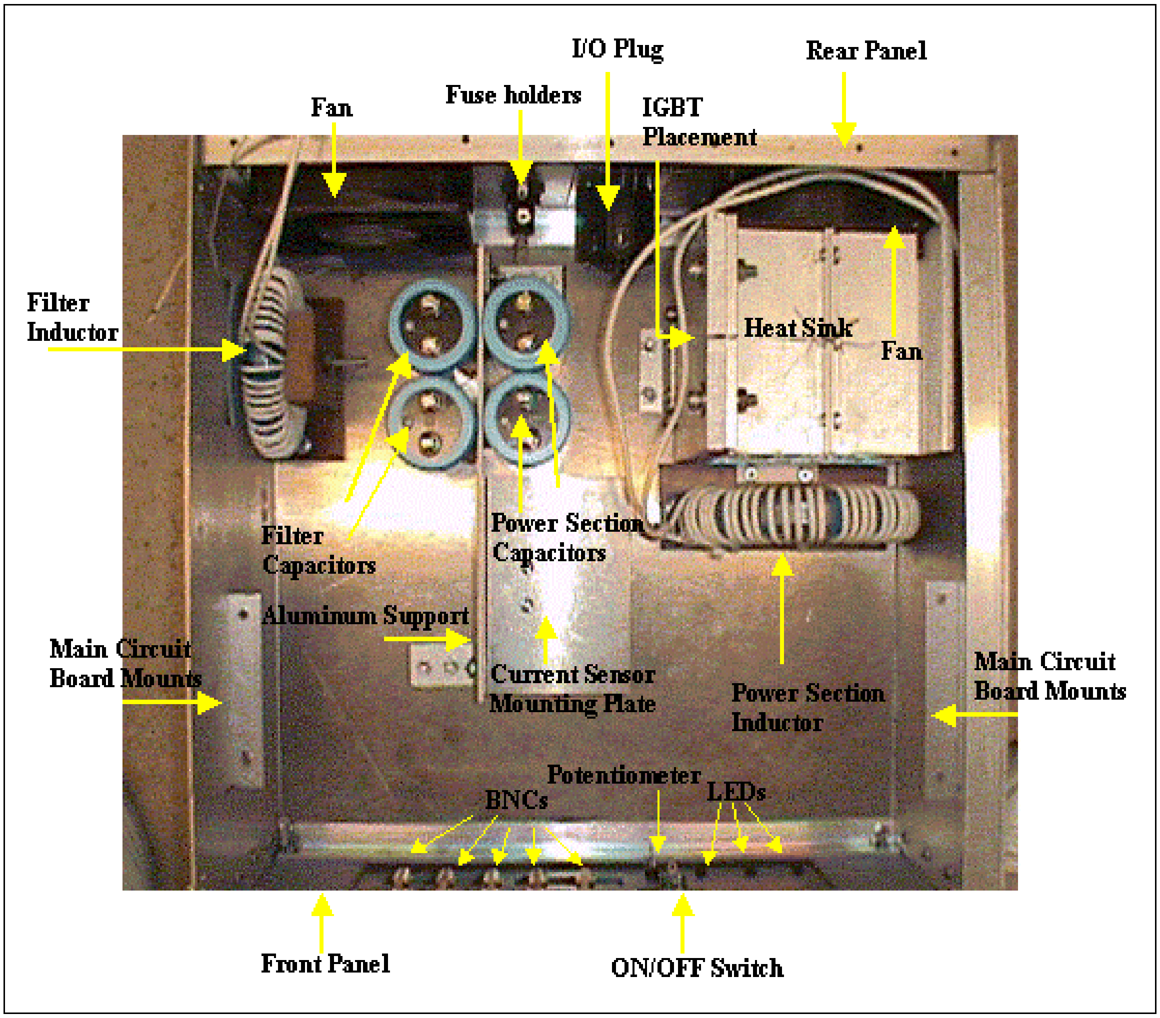


Figure 5-17, Heat Sink, Input Filter and Power Section Placement.

In Figure (5-18), the damping circuit is added to the input filter, the IGBT is installed onto the heat sink, the current sensor board platform is installed, and the platform brackets for the main circuit board are attached to the side of the cabinet. The IGBT has additional components attached to it (MOV and 2.2µF high frequency capacitors depicted in Figure (5-2)). Also illustrated, angled aluminum was placed along the perimeter of the SSCM to provide ruggedness and durability.

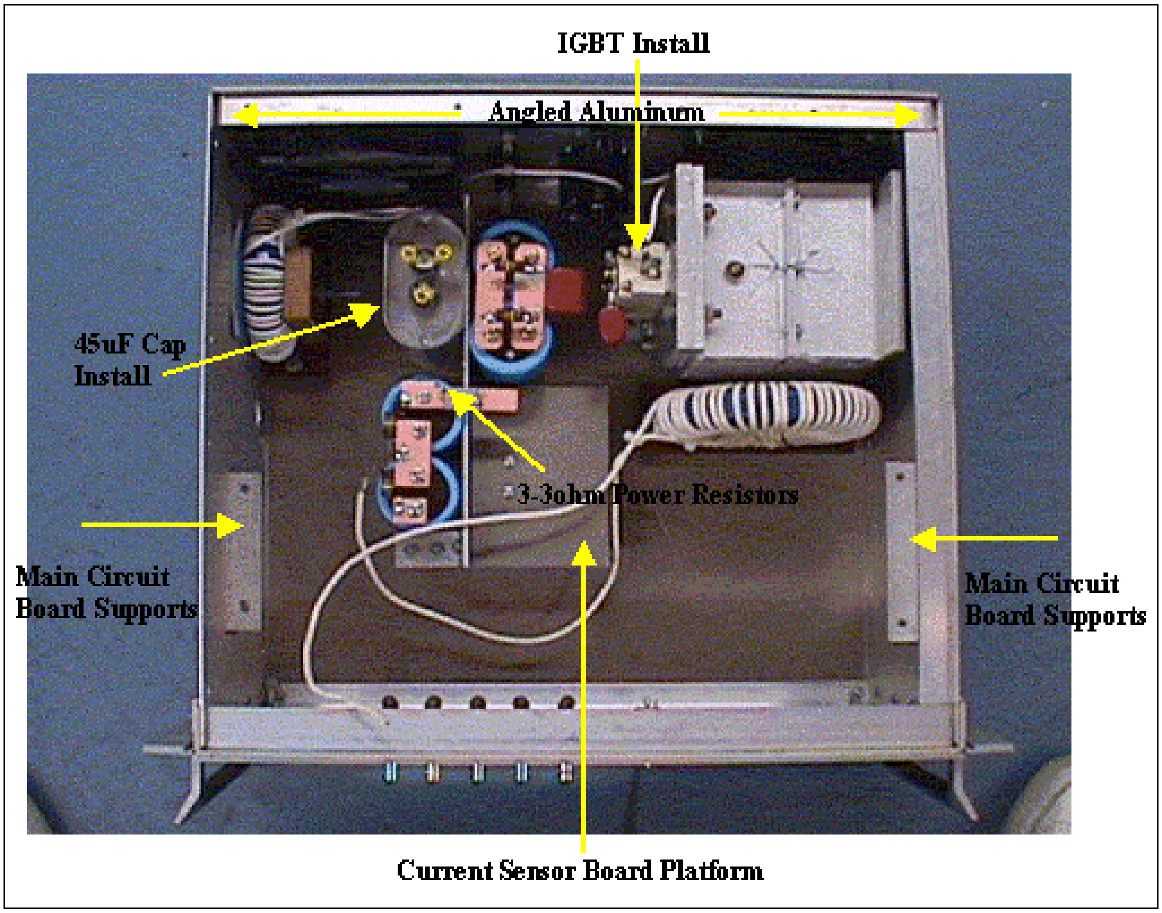


Figure 5-18, Input Filter Dampening Circuit and IGBT Install.

Figure (5-19) depicts the installation of the 115V/30V transformer, thermistor switch, and current sensor circuits. The wiring for the transformer and current sensors are labeled. Also pictured, the power section inductor is wired through the current sensor to the IGBT. Care was taken to ensure the wire was placed in the center of the current sensor aperture. The twisted pair wires from the current sensor boards feed J1CS (see Figure (5-2)). The thermistor wire also feeds J1CS pin 1 as seen in Figure (5-11). The transformer wiring is fed through the bottom of the main circuit board into J10AC.

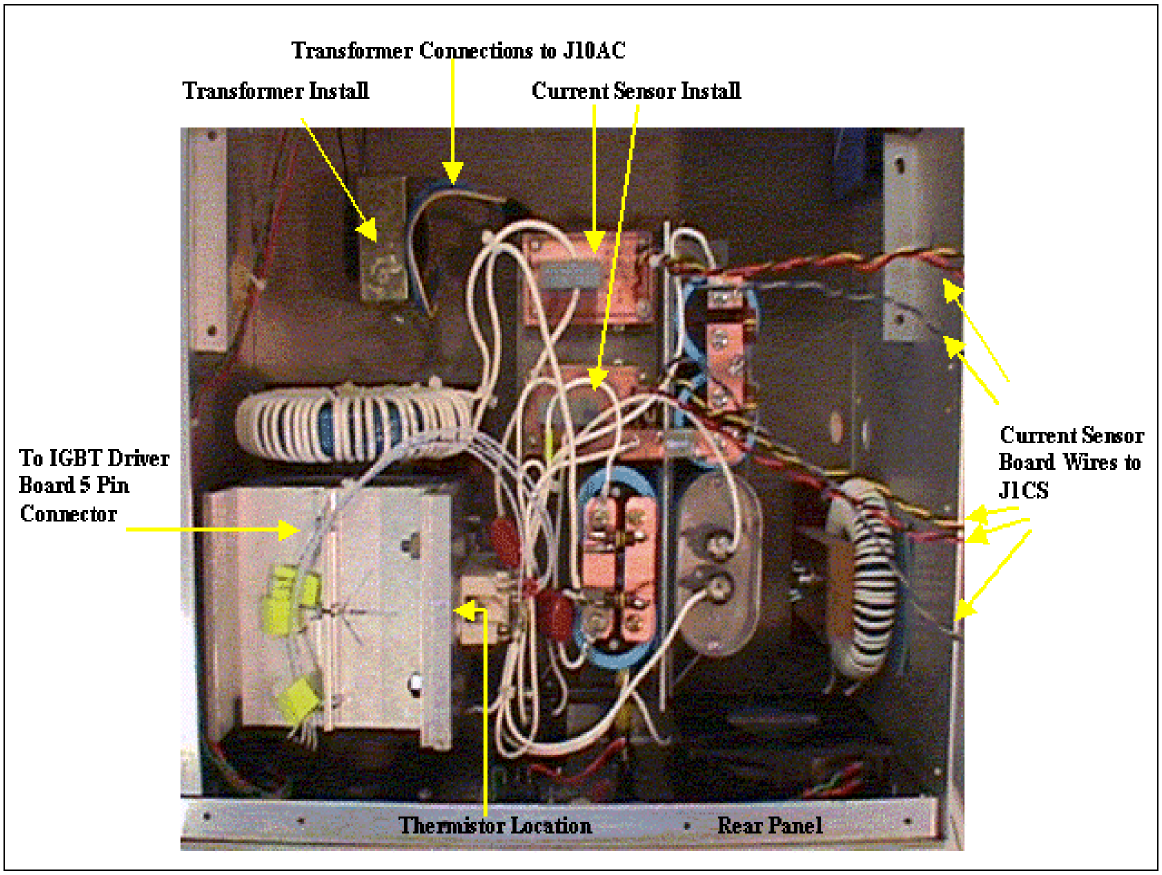


Figure 5-19, Transformer, Current Sensors, and Thermistor Install.

Figure (5-20) illustrates the installation of the digital meters, LEDs, and temperature and current reset pushbuttons. The 115V wiring comes in from the rear panel and connects to the on/off switch on the front panel. From the switch, 115V is routed to the transformer. In the upper right corner of Figure (5-20), elbows are attached to the BNC connectors to re-route the control signals (d(t), $i_L/5$, $i_o/5$, $V_{in}/100$, and $V_{out}/100$) to provide sufficient clearance for the main circuit board install. The BNC signal wires are routed underneath the main control board and connected to the main control board at connectors J4 through J8 as illustrated in Figure (5-12). The 1kΩ potentiometer functions to adjust the duty cycle from the front panel and is seen in the center of Figure (5-20). Also pictured, angled aluminum support is installed at the bottom of the SSCM to provide durability.

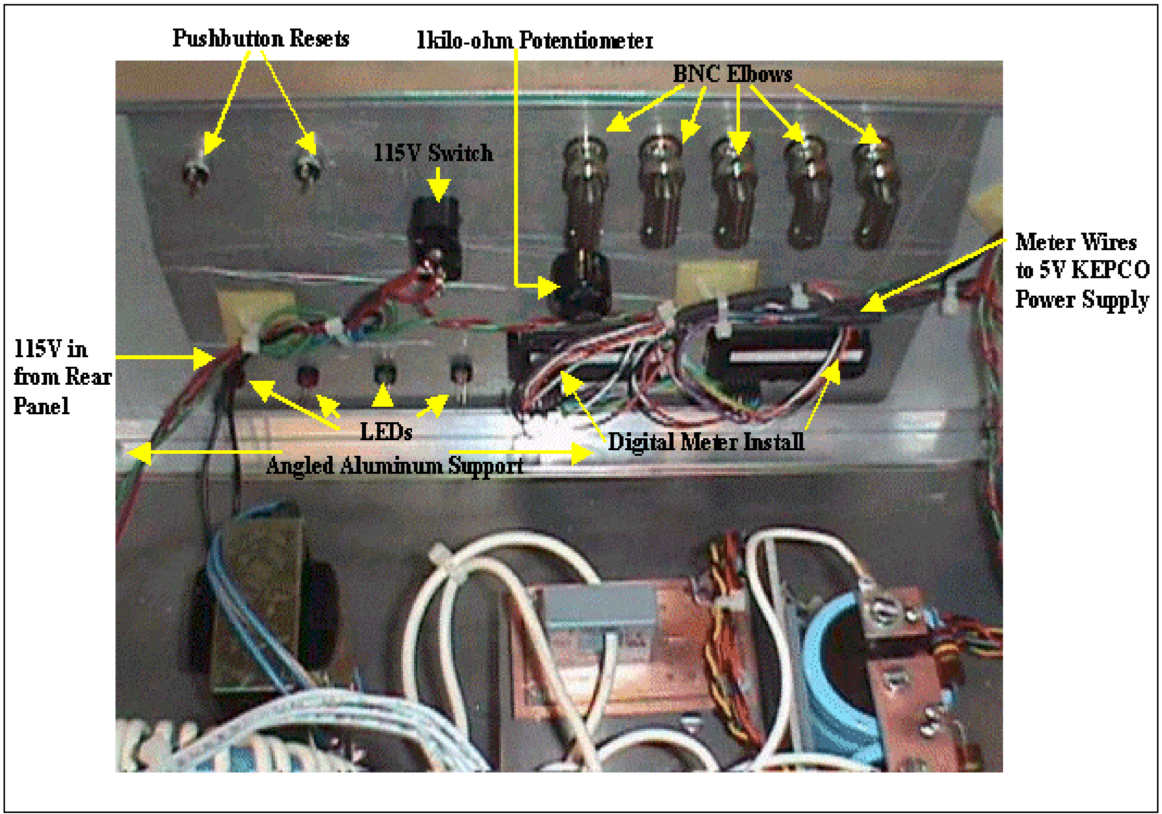


Figure 5-20, Meter, LED, and Pushbutton Install.

Figure (5-21) pictures the installation of the main circuit board and the IGBT driver board. The other end of the elbow BNC connectors from Figure (5-20) are routed underneath the main control board and connected to the top of the main circuit board as seen in Figure (5-21). This photo displays all connections to the main circuit board and IGBT driver board. The main circuit board houses the buffer stage, control stage, PWM stage, user select switch, voltage divider network, and protection and start-up circuitry. All connectors and circuits have been discussed and their detailed schematics provided in Chapter V. Table (5-1) summarizes of the connectors and circuits in the SSCM and provides the applicable figure number(s).

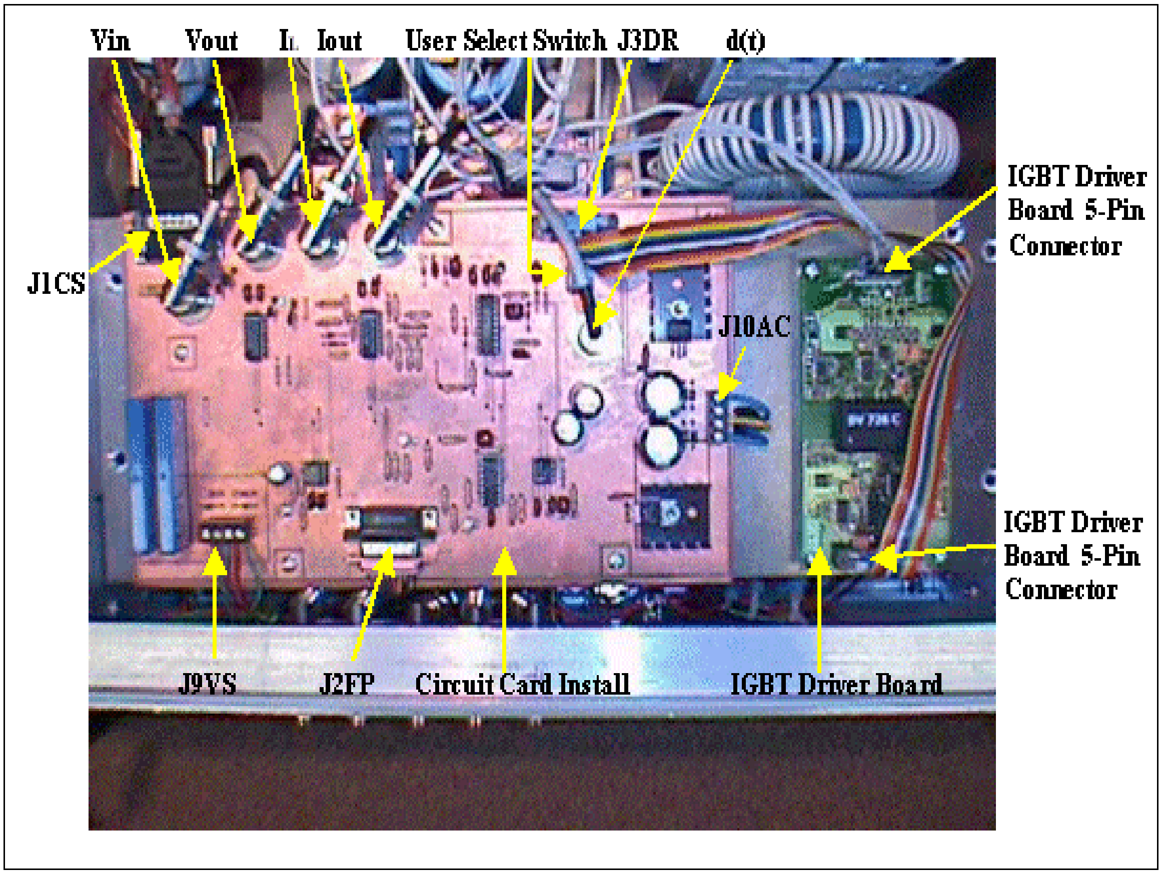


Figure 5-21, Main Circuit and IGBT Driver Board Install.

Connector/s or Circuit	Figure Number(s)
J1CS	5-2, 5-4, 5-6, 5-11, 5-14
J9VS	5-1, 5-3,
J2FP	5-10, 5-11, 5-15
J4-J8	5-6, 5-12
J3DR	5-8, 5-11, 5-13
J10AC	5-5
Voltage Sensing Circuit	5-1, 5-3
Current Sensing Circuit	5-2, 5-4
Main Circuit Board Power Supply	5-5
Buffer Stage	5-6
Main Control Stage	5-7
User Select Switch	5-8
PWM Stage	5-9
Protection and Start-up Circuitry	5-10, 5-11

Table 5-1, Summary of SSCM Figures.

E. SUMMARY

The purpose of this chapter was to compile and document the detailed schematics of the final product. Many schematics were contained in Chapters II-IV, but their purpose was mainly illustrative. Although correct, previous chapter schematics did not contain all of the detail required to duplicate the SSCM fabrication at a future date. In Chapter VI, detailed testing is documented to validate the SSCM operation.

VI. TESTING AND VALIDATION

A. PURPOSE

The purpose of this chapter is document all test results conducted on the SSCM. All testing was accomplished at NPS with available lab equipment.

B. BACKGROUND

Prior to final assembly, each of the following circuits were bread-boarded and tested:

- Control circuit,
- PWM circuit,
- Protection and start-up circuitry.

The control circuit, discussed in Chapter IV, was simulated using the hardware-in-the-loop capabilities of the dSPACE 1103 development system [24]. To test the control circuit, an average-value model of the converter was simulated in SIMULINK and the bread-boarded control circuit was interfaced with the dSPACE controller board. In dSPACE, R_{load} was placed on a slider (load was varied between 20Ω and 200Ω) and $i_o/5$, $i_L/5$, and $V_{out}/100$ were outputted from dSPACE to the control board. $V_{in}/100$ was simulated using a power supply set to 4V (simulated 400V reference). Duty cycle was generated by the control board and fed back to dSPACE for display (see Appendix A). R_{load} was varied throughout its entire range to verify that the control board maintained a stable 0.8 duty cycle.

To test the PWM circuit, a power supply (supplying 8V to simulate a 0.8 duty cycle) was connected to the input of the PWM chip (U3 pin 11). The PWM breadboard circuitry produced $\approx$20.4kHz signal at pin 4 of U3, well within design specifications. Detailed procedures on dSPACE operation are offered in Appendix E. Once each sub-circuit was validated for its particular function, final assembly took place.

C. TESTING

The following tests were performed on the SSCM:

- Full load ($\approx 20\Omega$),
- Minimum loading ($\approx 200\Omega$),
- Continuous mode,
- Discontinuous mode,
- Transient response,
- Efficiency.

As previously mentioned, all test equipment was available in the NPS Power Systems lab. Table (6-1) lists all equipment utilized in the testing phase and Figure (6-1) illustrates the test circuit set up in the lab.

Equipment	Parameters	Manufacturer	Part or Model Number
Variac	3-phase/35A/60Hz 480V input/0-560Voutput	Staco Energy Products	6020-3Y
Power Diode Rectifier	50A	INVERPower controls LTD	P101 DM
2-Filter Capacitors	10,000 MFD 350 WVDC	INVERPower controls LTD	P106 FC
Resistor Load (3 banks)	3kW-115V	INVERPower controls LTD	P108-RL
Voltage Source Inverter (used in transient analysis)	3-phase	INVERPower controls LTD	P108-RL
2-non-Inductive Shunts	0.0010127Ω/20W 0.0010123Ω/20W	INVERPower controls LTD	P109-NIS S/N P109-023
6-Pulse Amplifier (used in transient analysis)	+24V/-15V	INVERPower controls LTD	L100 AM
Fluke Meters	8060A Multimeter	Fluke	8060A
Oscilloscope	60MHz	Tektronix	2212

Table 6-1, Required Test Equipment.

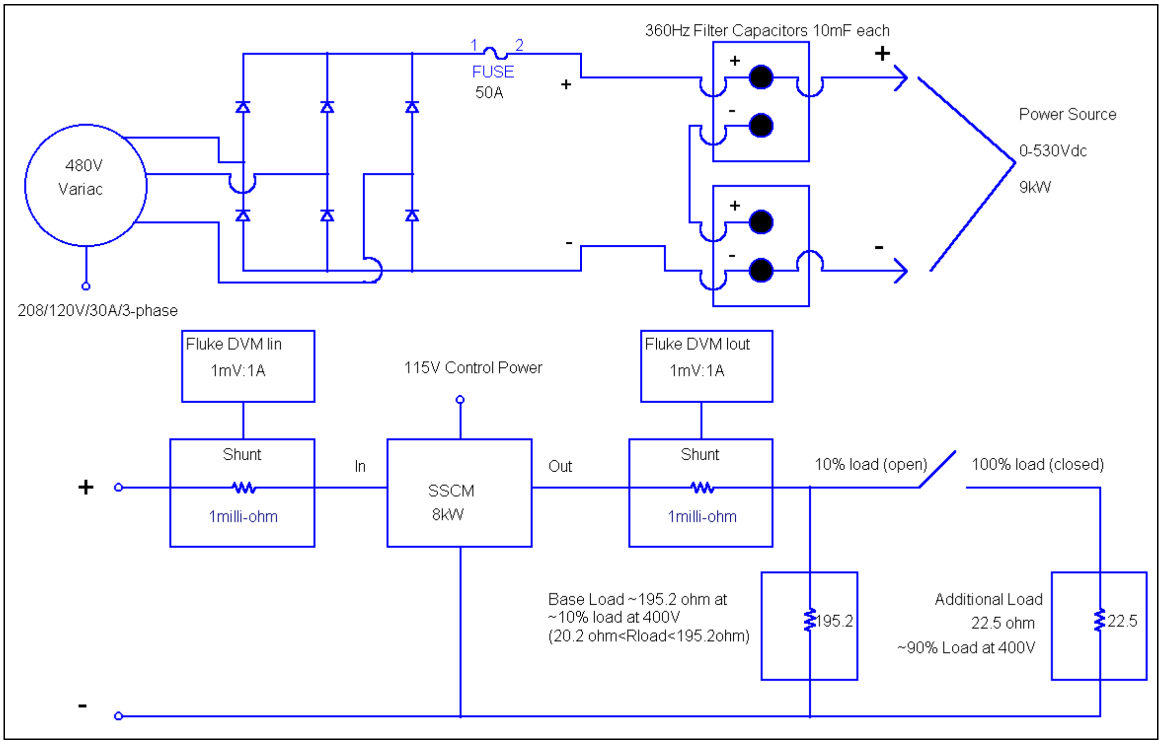


Figure 6-1, Test Circuit.

1. Full-Load Testing

Full-load testing was performed and the data recorded is presented in Table (6-2). The purpose of this test was to assure that the SSCM performed as designed at approximately full power for different commanded output voltages. The circuit at the bottom right of Figure (6-1) provides $R_L \approx 20.2\Omega$ (switch closed). Prior to testing, the load banks measured at 195.2Ω and 22.5Ω, respectively, giving a total parallel combination of 20.2Ω.

The variac in Figure (6-1) was slowly raised from 0V to 500V. Slight adjustment of the variac was required as V_{out} was incrementally increased from $\approx$100V up to $\approx$425V by adjusting the duty cycle (front panel potentiometer). All testing commenced at V_{out}=100V and E=500V. Table (6-2) lists all values recorded and the measured efficiency at each voltage level. Observed efficiencies were as expected in that the IGBT was expected to dissipate $\approx$100W at full power. Switching losses in the IGBT and

conduction losses accounted for the efficiencies being less than ideal (100%). Power loss observed in the full-load testing phase is listed in Table (6-3). No significant heat ($\approx$95°F) was generated in the power section inductor or the heat sink (was able to place hand on heat sink for the length of testing). Voltages were measured across the IGBT collector-emitter (V_{CE}) and currents were measured through the inductor (I_L). Five oscilloscope printouts were obtained at maximum loading ($\approx 19.7\,\Omega$ measured) and are labeled Figures (6-2 through 6-6). As indicated by the measured output voltage and current recorded in Table (6-2), the effective output load resistance ranged from 19.78Ω to 19.63Ω.

In Figures (6-2) through (6-4), the inductor is in the continuous conduction mode of operation (the inductor current I_L does not go to zero) and all waveforms are as expected. In Figures (6-5) and (6-6), at higher output power the charging and discharging of the inductor current is no longer linear. This is an expected condition. As current is increased through the inductor, the effective permeability decreases in a nonlinear fashion as seen in the B-H curve in Appendix A. From initial core design efforts, the expected worst decay in inductance from no-load to full-load is $\approx$50% reducing the 1mH inductor to $\approx$500μH. Using Figure (6.2) ($\approx$25% load) and Figure (6.5) ($\approx$100% load), an estimate of the reduction in inductance can be made using Equation (6-1) with $V_c = V_{out}$, $E = V_{in}$, $D = 0.8$, $T = 50$μsec, and ΔI pulled from the respective figures.

$$L = \left(\frac{E - V_c}{\Delta I} \right) DT \tag{6-1}$$

At 25% load $\Delta I_L = 4.3$A and at 100% load $\Delta I_L = 9$A which corresponds to 930μH and 440μH, respectively. Considering the no-load case is 1mH, the degradation in inductance is 7% at 25% load and 56% at 100% load. Thus, the theoretical analysis from Chapter III section B1 appears confirmed.

Figure Number	V_{in} Volts	V_{out} Volts	I_{in} Amps	I_{out} Amps	P_{in} Watts	P_{out} Watts	Efficiency Percent
6-2	500.3	100.5	1.13	5.08	565.3	510.5	90.3
6-3	500.0	200.0	4.24	10.14	2120.0	2028.0	95.6
6-4	500.1	300.2	9.38	15.28	4690.9	4587.1	97.8
6-5	500.2	400.3	16.52	20.39	8263.3	8162.12	98.7
6-6	528.2	425.0	17.62	21.65	9306.9	9201.25	98.9

Table 6-2, Full Load at 19.7 ohms (100% Load).

Figure Number	P_{in} Watts	P_{out} Watts	Power Loss Watts
6-2	565.3	510.5	54.8
6-3	2120.0	2028.0	92.0
6-4	4690.9	4587.1	103.8
6-5	8263.3	8162.12	101.2
6-6	9306.9	9201.25	105.6

Table 6-3, Power Loss in Converter.

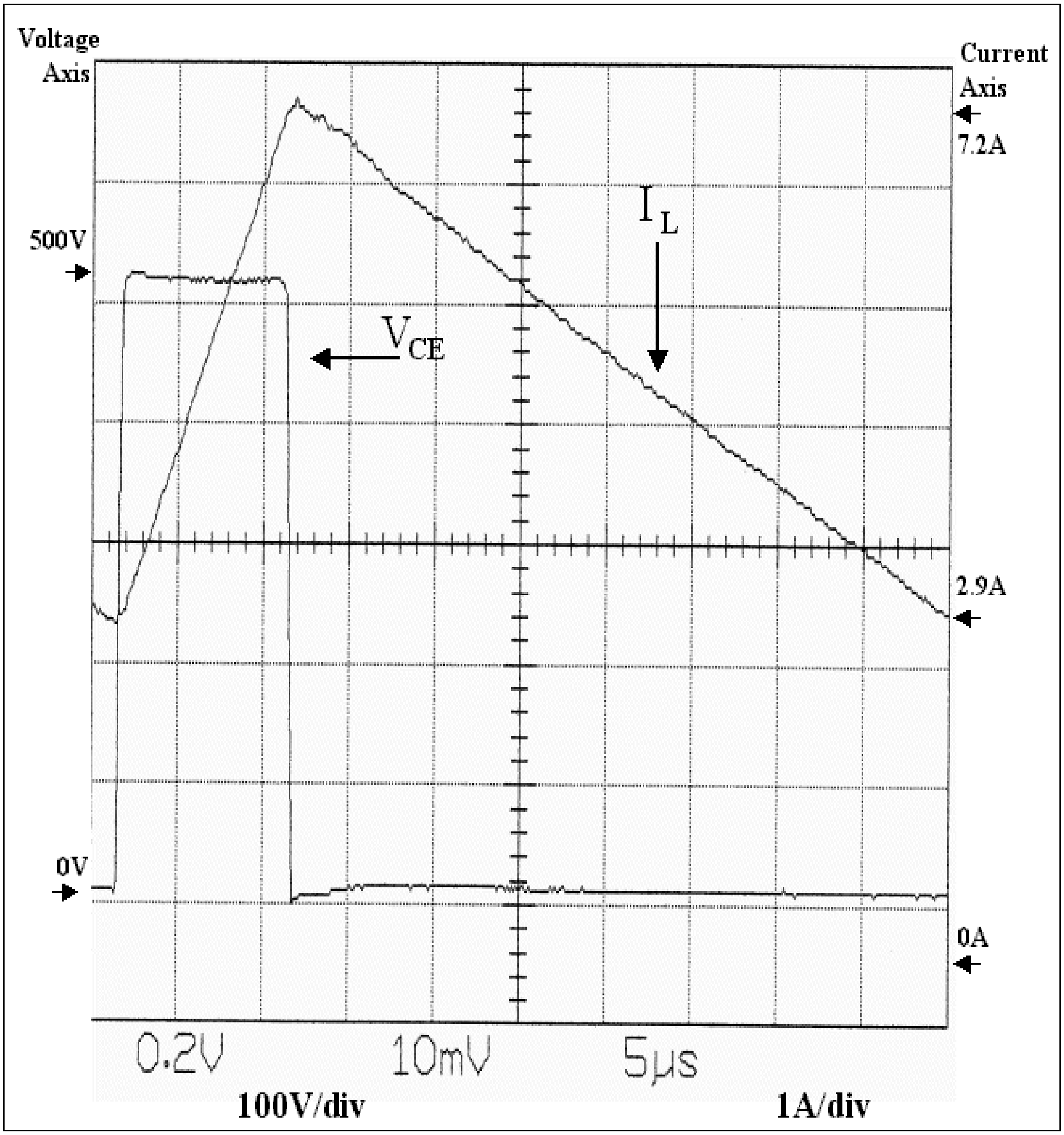


Figure 6-2, Voltage across the IGBT (V_{CE}) and Current through the Inductor (I_L) for one Switching Cycle with V_{in} = 500.3V, V_{out} = 100.5V and R_{Load} = 19.78Ω (measured at 20.2Ω with zero current).

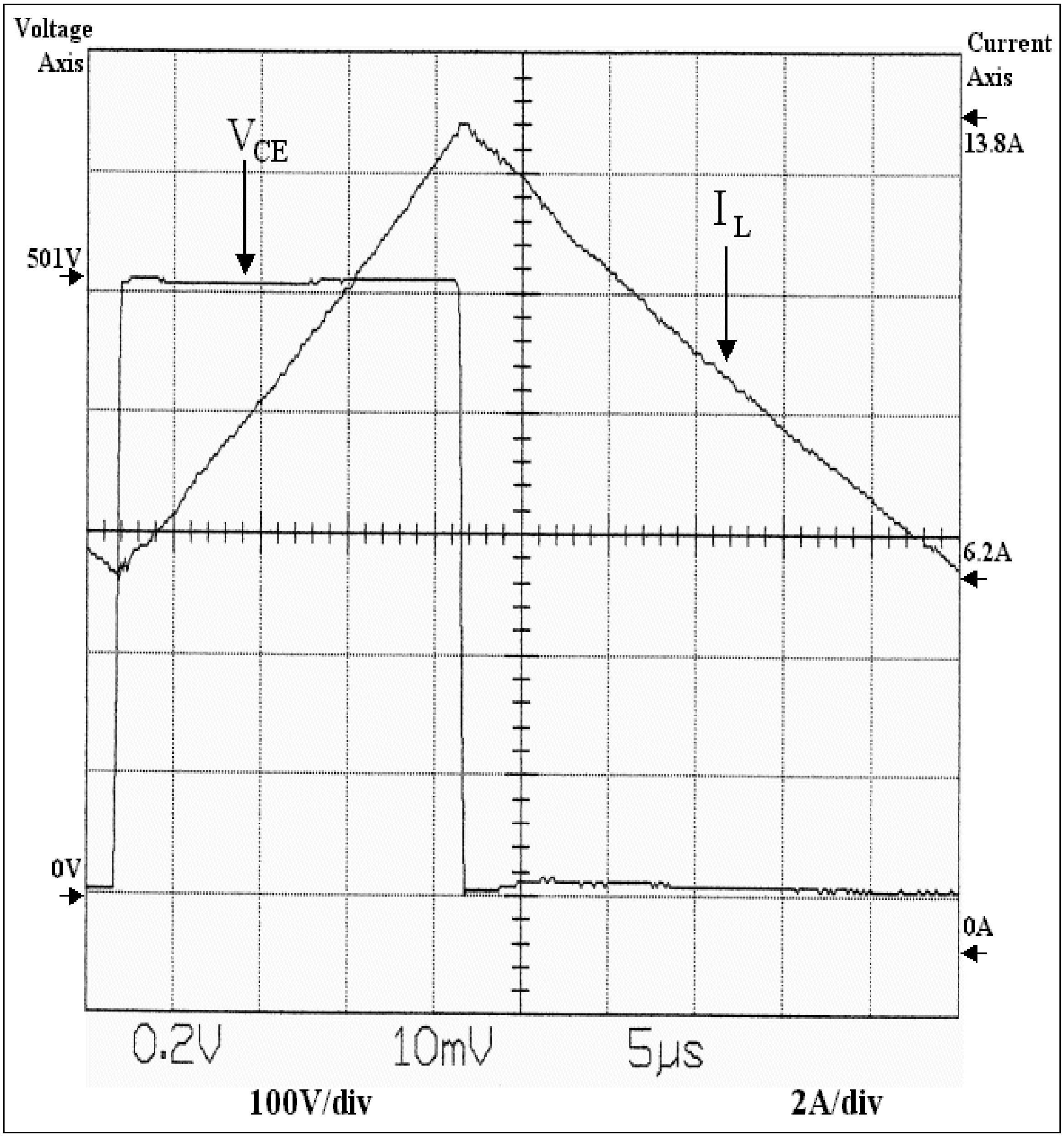


Figure 6-3, Voltage across the IGBT (V_{CE}) and Current through the Inductor (I_L) for one Switching Cycle with V_{in} = 500.0V, V_{out} = 200.0V and R_{Load} = 19.72Ω (measured at 20.2Ω with zero current).

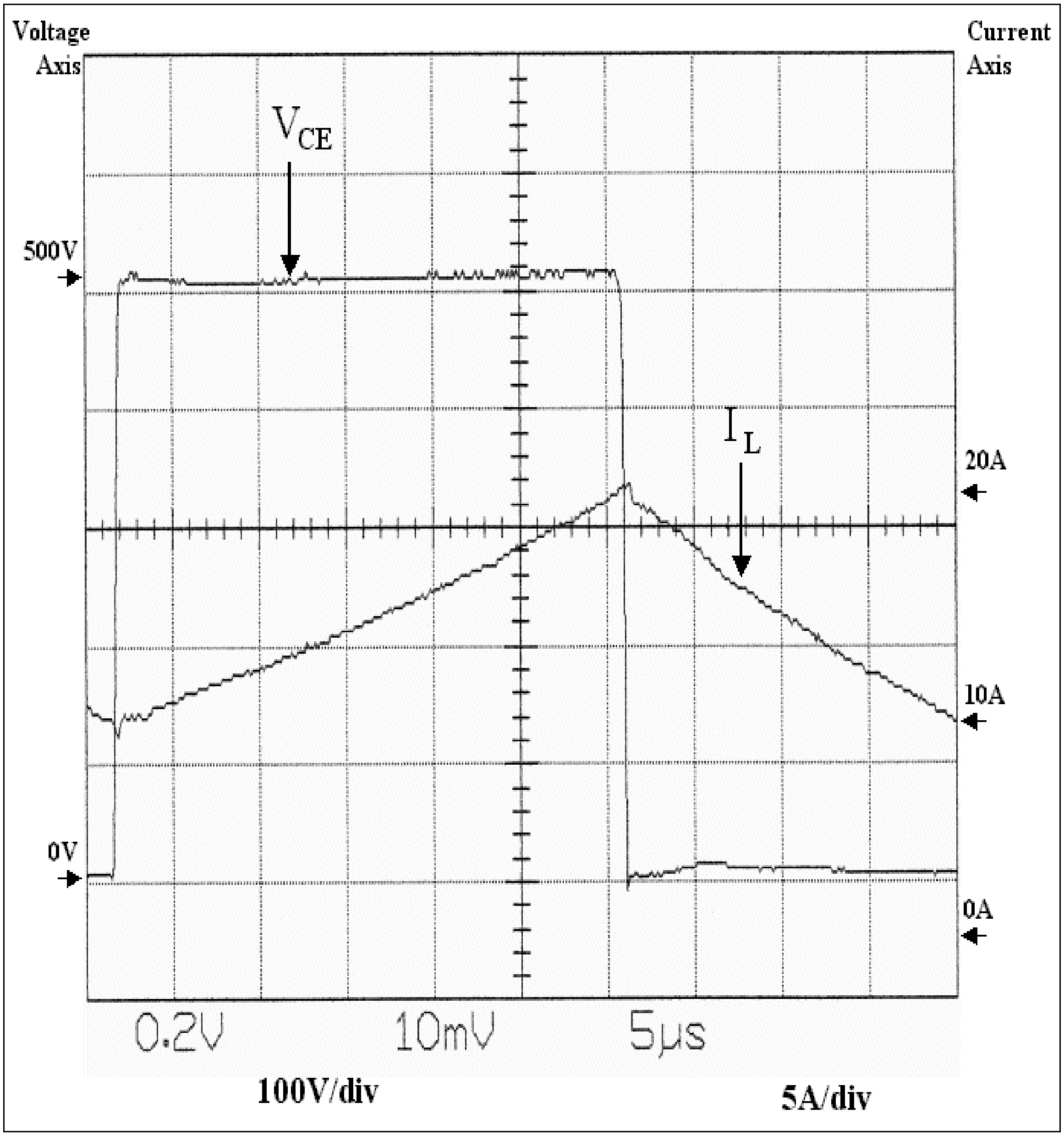


Figure 6-4, Voltage across the IGBT (V_{CE}) and Current through the Inductor (I_L) for one switching cycle with V_{in} = 500.1V, V_{out} = 300.2V and R_{Load} = 19.65Ω (measured at 20.2Ω with zero current).

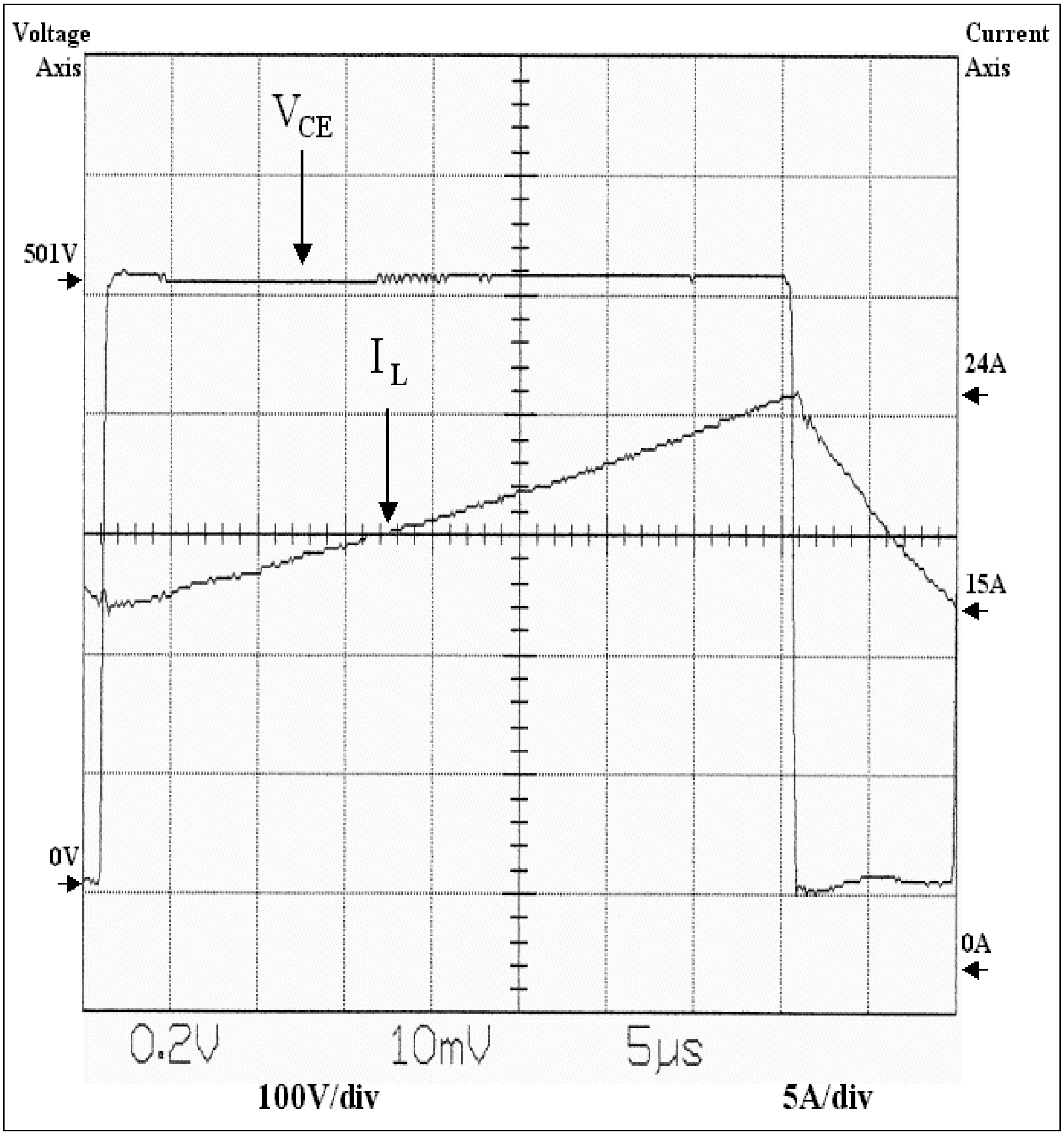


Figure 6-5, Voltage across the IGBT (V_{CE}) and Current through the Inductor (I_L) for one Switching Cycle with V_{in} = 500.2V, V_{out} = 400.3V and R_{Load} = 19.63Ω (measured at 20.2Ω with zero current).

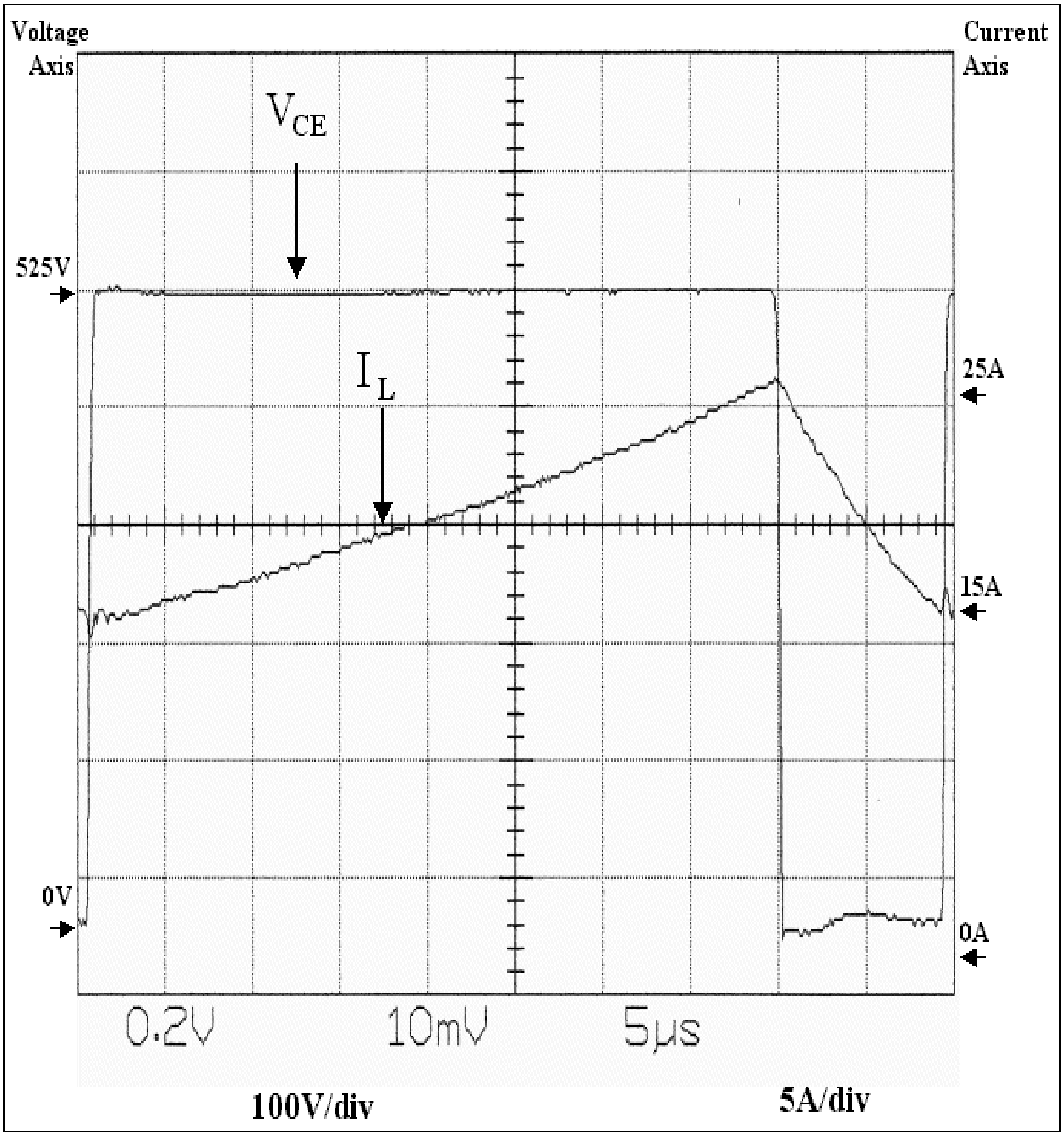


Figure 6-6, Voltage across the IGBT (V_{CE}) and Current through the Inductor (I_L) for one Switching Cycle with V_{in} = 528.2V.4, V_{out} = 425V and R_{Load} = 19.63Ω (measured at 20.2Ω with zero current).

2. Minimum-Load Testing

Minimum-load testing was performed and the data recorded is presented in Table (6-4). As stated in the full-load test, the variac provided the input voltage at 500V. V_{out} was increased from $\approx$ 100V up to $\approx$ 400V by adjusting the duty cycle (front panel potentiometer). Table (6-4) lists all values recorded and the measured efficiency at each voltage level. Losses in the IGBT/diode package (conduction and switching losses) and power consumed in the inductor accounted for most of the losses causing efficiencies to be less than 100%. The IGBT was the only component that produced any heat (only warm to the touch) all other components remained at essentially room temperature. Power loss observed in the testing phase is listed in Table (6-5). For plotting purposes, voltages were measured across the IGBT collector-emitter (V_{CE}) and currents were measured through the inductor (I_L). Five oscilloscope printouts were obtained at minimum loading ($\approx 193\,\Omega$) and are labeled Figures (6-7 through 6-11).

Because the converter was designed to operate in continuous conduction mode with a minimum load of $R_L = 200\Omega$ at D = 0.8, much of this testing was done in the discontinuous mode as seen in Figures (6-7) through (6-9). Figure (6-10) depicts the barely continuous mode while Figure (6-11), D = 0.8, shows the converter in its designed minimum load condition. Figure (6-11) can be used to estimate the near no-load value of the main inductor at 1mH (where $\Delta I \approx$ 4A).

Of most interest though, is the minimally damped $\approx$175kHz oscillation (5.7μsec period) that appears in Figures (6-7) through (6-9). This "ringing" between the main inductor and IGBT body capacitance is not destructive and is actually most useful in estimating the value of the IGBT body capacitance ($C_{IGBT} \approx$ 826pF close to the specification sheet of 720pF-900pF). If a snubber had been used on the IGBT/diode, this ringing would have been eliminated at the cost of substantial higher converter losses. Since the ringing takes place only under discontinuous mode and never exceeds the IGBT or diode voltage or current specifications, it is simply an anomaly of the snubberless design. Additionally, the 1200V/100A IGBT is protected with a 1100V MOV (Metal Oxide Varistor).

Figure Number	V_{in} Volts	V_{out} Volts	I_{in} Amps	I_{out} Amps	P_{in} Watts	P_{out} Watts	Efficiency Percent
6-7	500.1	100.3	0.14	0.52	70.01	52.16	74.5
6-8	501.0	200.0	0.47	1.04	235.47	208.00	88.3
6-9	500.4	300.5	1.00	1.56	500.40	468.78	93.7
6-10	500.7	376.2	1.53	1.95	766.07	733.59	95.8
6-11	500.8	400.1	1.72	2.07	861.38	828.21	96.1

Table 6-4, Minimum Load at $\approx$193 ohms ($\approx$10% Load).

Figure Number	P_{in} Watts	P_{out} Watts	Power Loss Watts
6-7	70.01	52.16	17.85
6-8	235.47	208.00	27.47
6-9	500.40	468.78	31.62
6-10	766.07	733.59	32.48
6-11	861.38	828.21	33.17

Table 6-5, Power Loss in Converter.

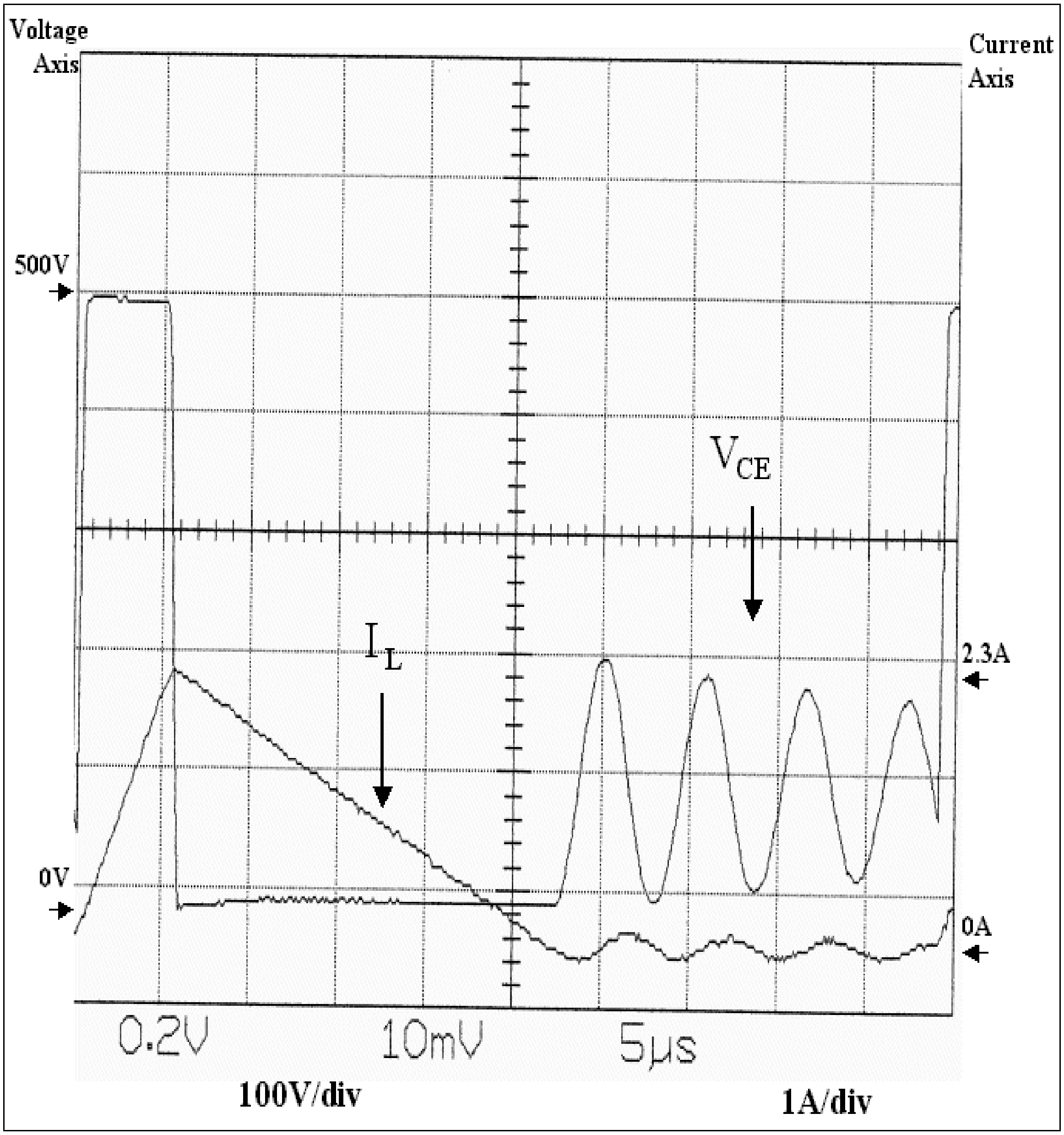


Figure 6-7, Voltage across the IGBT (V_{CE}) and Current through the Inductor (I_L) for one Switching Cycle with V_{in} = 500.1V, V_{out} = 100.3V and $R_{Load} \approx$ 192.8Ω.

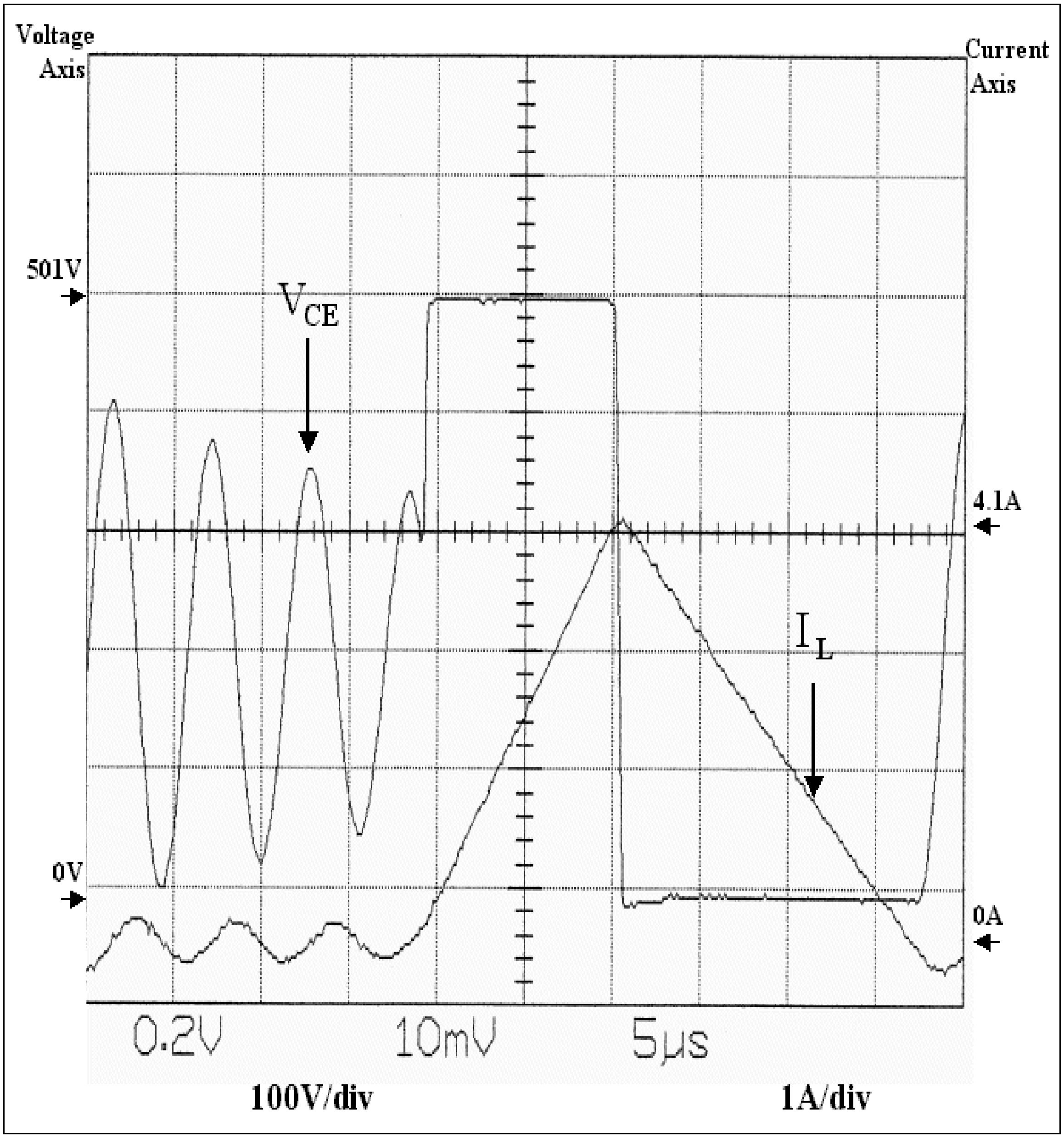


Figure 6-8, Voltage across the IGBT (V_{CE}) and Current through the Inductor (I_L) for one Switching Cycle with V_{in} = 501.0V, V_{out} = 200.0V and $R_{Load} \approx$ 192.8Ω.

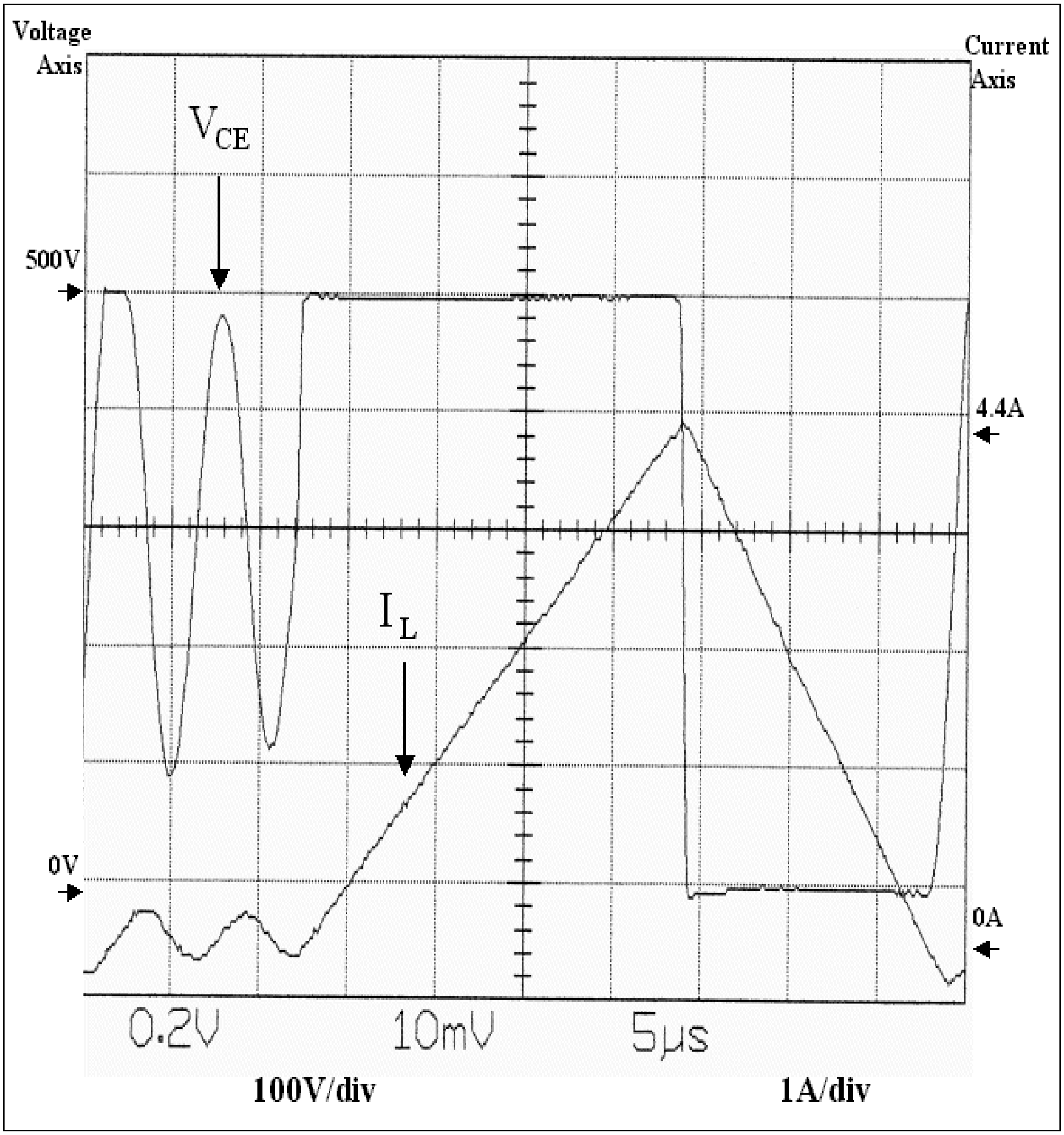


Figure 6-9, Voltage across the IGBT (V_{CE}) and Current through the Inductor (I_L) for one Switching Cycle with V_{in} = 500.4V, V_{out} = 300.5V and $R_{Load} \approx$ 192.8Ω.

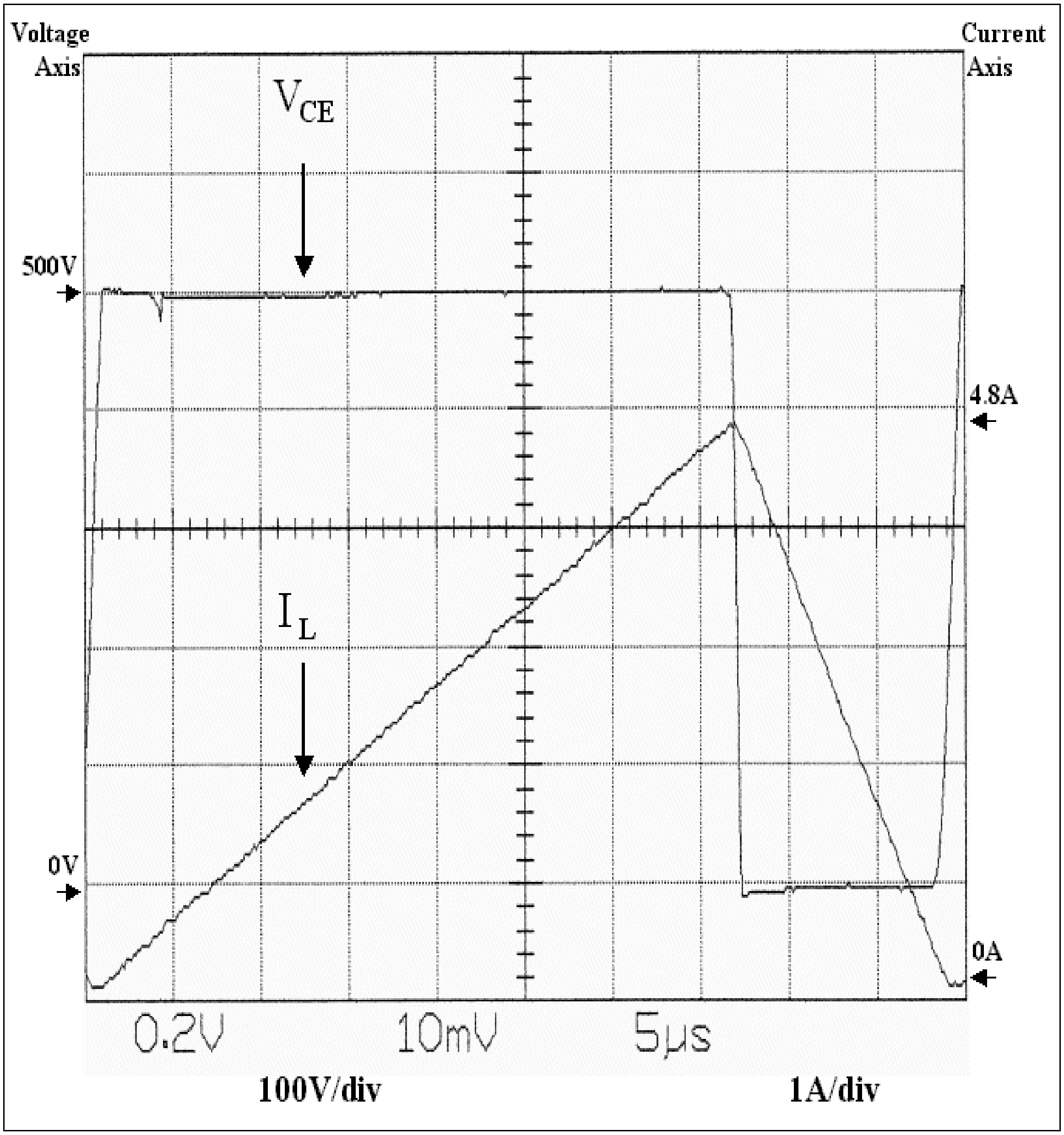


Figure 6-10, Voltage across the IGBT (V_{CE}) and Current through the Inductor (I_L) for one Switching Cycle with V_{in} = 500.7V, V_{out} = 376.2V and $R_{Load} \approx$ 192.8Ω.

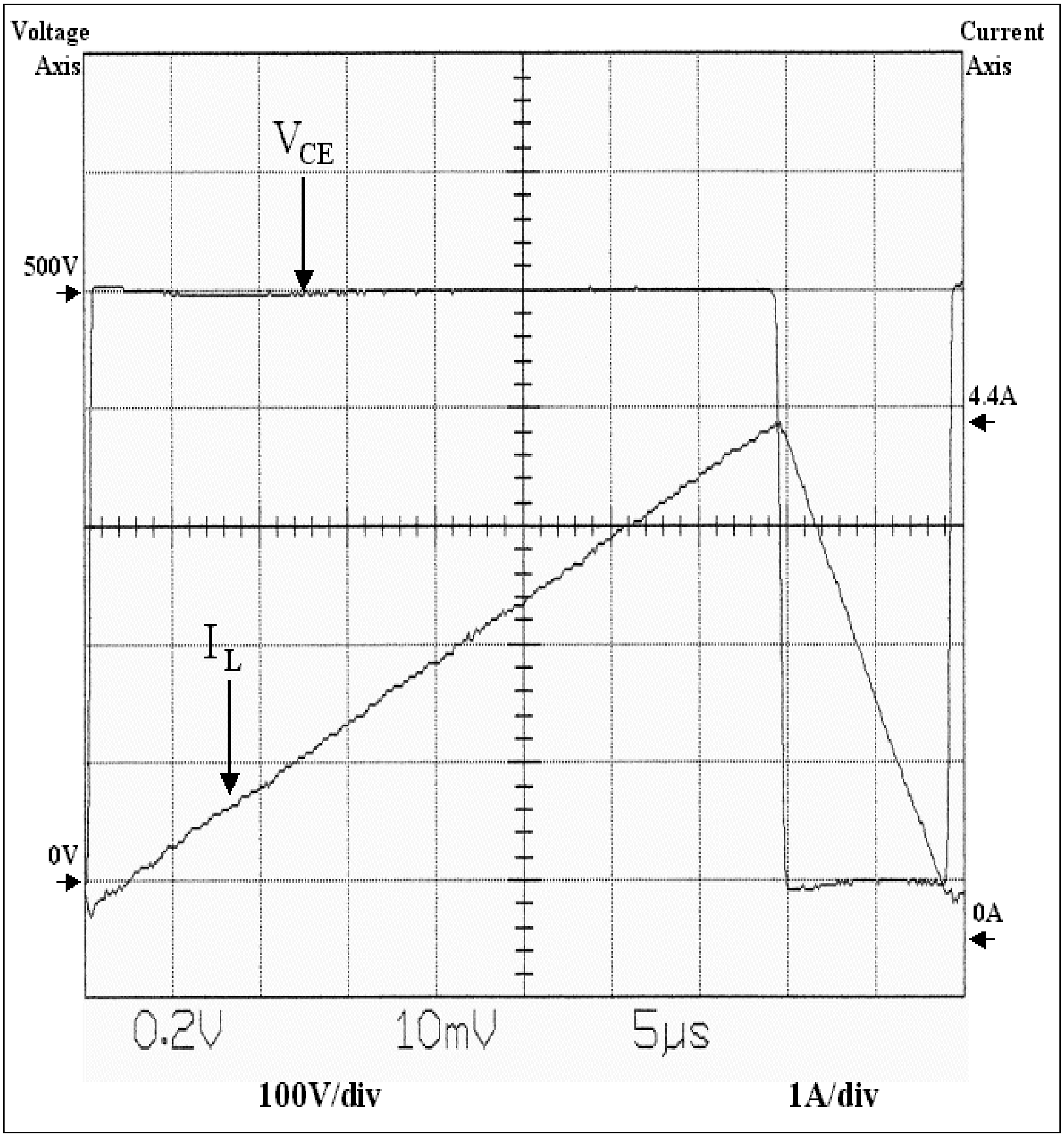


Figure 6-11, Voltage across the IGBT (V_{CE}) and Current through the Inductor (I_L) for one Switching Cycle with V_{in} = 500.8V, V_{out} = 400.1V and R_{Load} $\approx$ 192.8Ω.

3. Transient-Analysis Testing

The purpose of this section is to compare laboratory transient results with that of the SIMULINK transient results (Appendix B contains the MATLAB code and detailed SIMULINK model). The transient test was setup as illustrated in Figure (6-12). To ensure accuracy during testing, the actual loads used in the lab equaled the loads used in the simulation to within $\pm 0.21\Omega$.

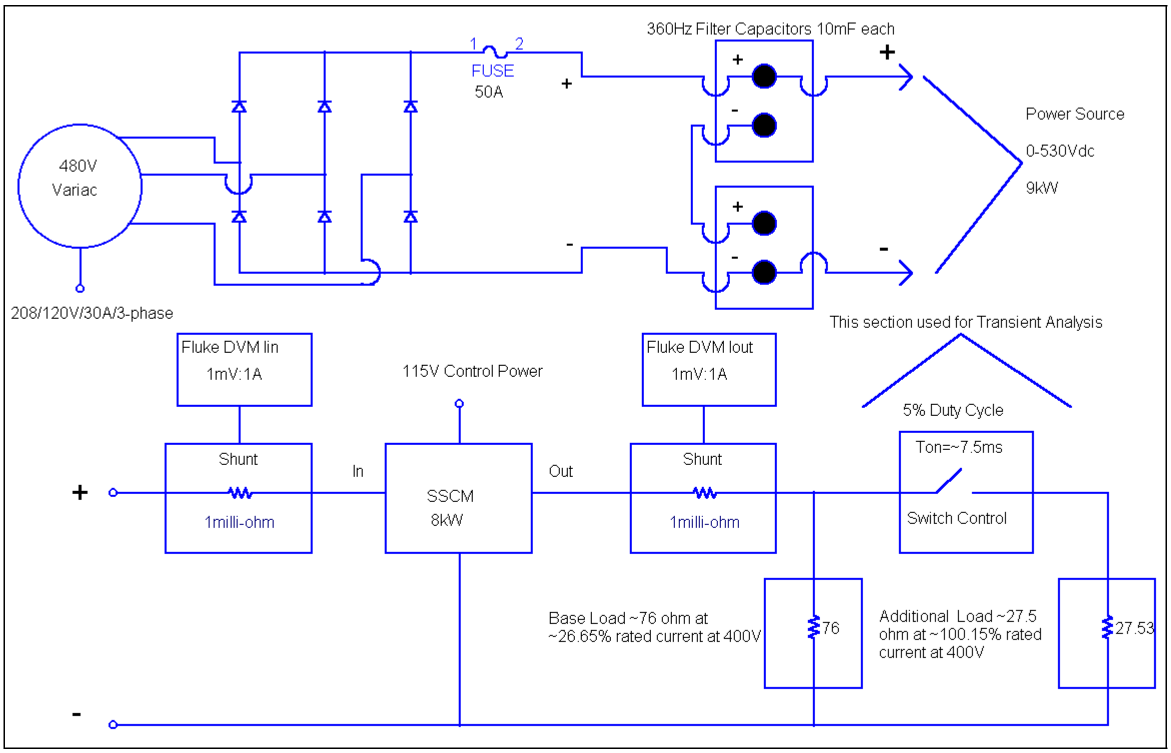


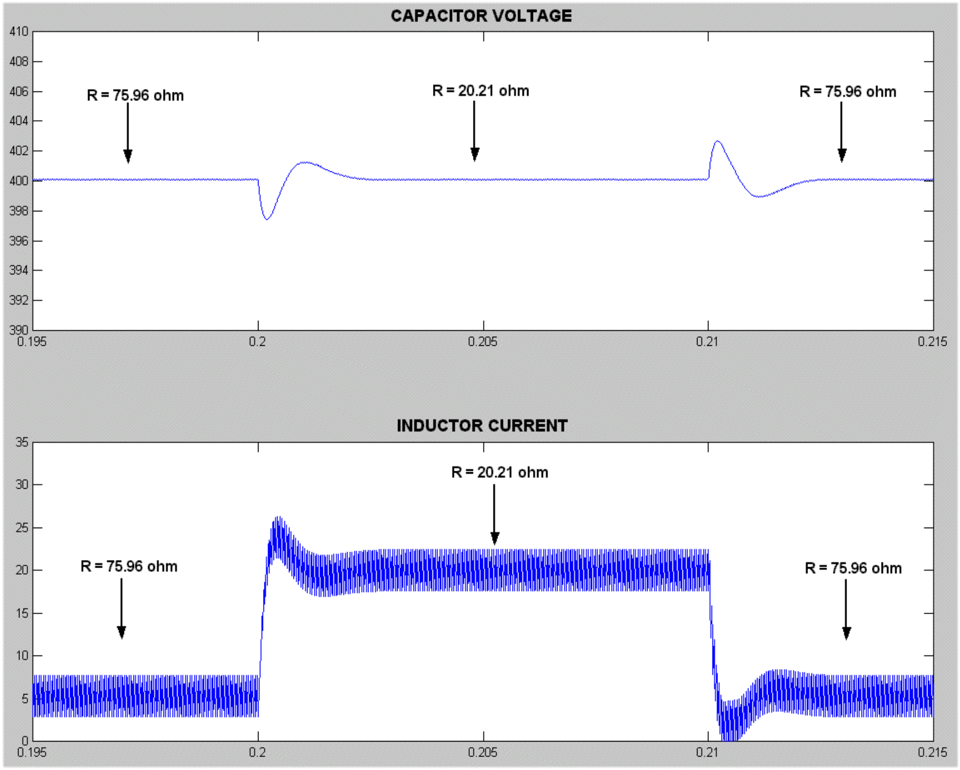
Figure 6-12, Transient Analysis Test Circuit.

Before starting the transient test, the two load conditions for transient analysis were documented in Table (6-6). Once the test conditions were established, the load was switched from 76Ω to 20Ω to 76Ω while maintaining an output voltage of $\approx$ 400V. Switching the load in this manner provided a 26.65% rated current flow at 76Ω and a 100.15% rated current flow at 20.21Ω. As can be observed in Figure (6-13), the output voltage transient is $\approx \pm 3$V for the simulation and $\approx \pm 5$V for the actual converter. The waveform shapes reasonably match except for the inductor current step to full load. The

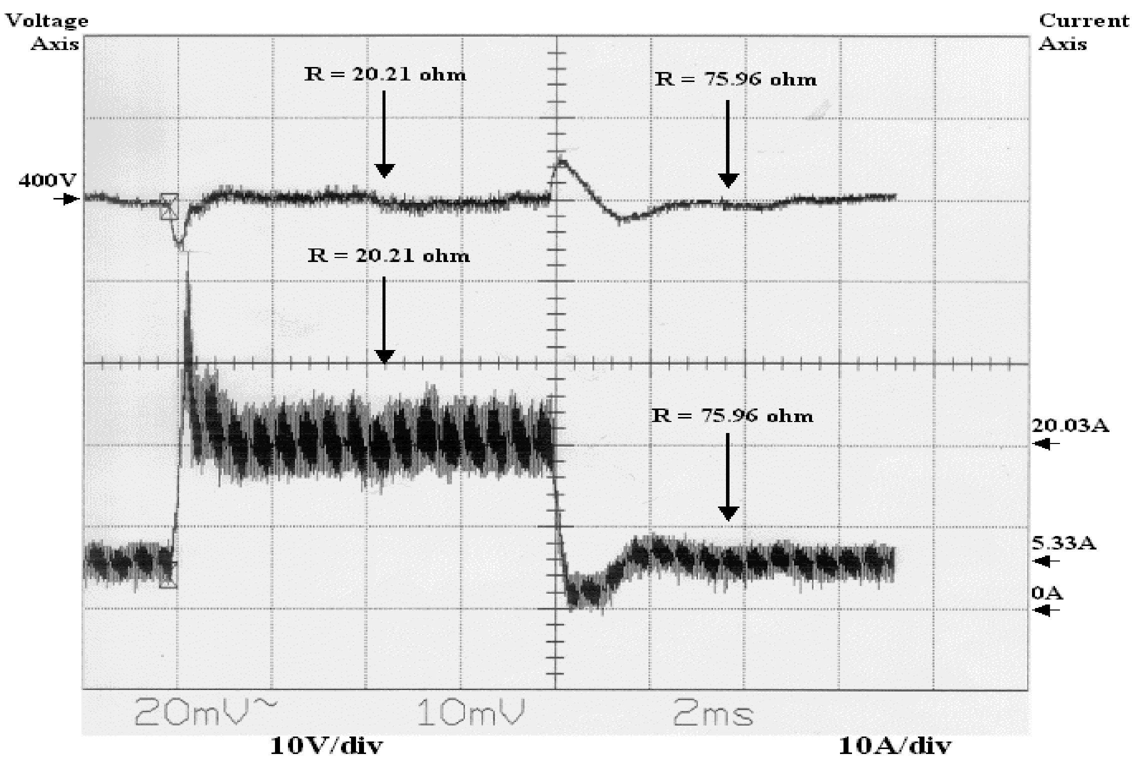
much larger transient in the inductor is thought to be due to the more than 50% loss in inductance at full load (which is not currently incorporated in the simulation).

Figure Number	**Transient Step**	**V_{in} Volts**	**V_{out} Volts**	**I_{in} Amps**	**I_{out} Amps**	**P_{out} Watts**	**R_{LOAD}**
6-13	1	528.1	404.9	4.32	5.33	2158.12	75.96Ω
6-13	2	472.5	404.9	17.84	20.03	8110.15	20.21Ω

Table 6-6, Transient Analysis.



Part A Simulation Results



Part B Experimental Results

Figure 6-13, Voltage across the Capacitor (V_{out}) and Current through the Inductor (I_L) for V_{in} = 528.1V, V_{out} = 404.9V and 20.21Ω $\leq R_{Load} \leq$ 75.96Ω ± 5%.

D. SUMMARY

This chapter outlined the test results on the SSCM found in the laboratory and through simulation. The following tests were conducted on the SSCM in the lab to verify proper operation:

- over-current time-out,
- over-temperature shutdown,
- pulse-by-pulse current limiting,
- full-load testing (complete duty cycle range),
- minimum-load testing (complete duty cycle range),
- pushbutton reset operation,
- airflow through unit and heat generated (minimal),
- transient analysis and,
- discontinuous operation.

In Chapter VII, conclusions and accomplishments in the design project are addressed as well as possible future work in this area.

VII. CONCLUSIONS

A. SUMMARY OF FINDINGS

This research documented the design and construction of an 8kW dc-dc converter. The converter will be placed into a larger testbed for a small-scale Integrated Power System (IPS) to be assembled by ESAC. The key areas covered in the thesis are:

- Detailed schematics,
- Detailed component parts/manufactures lists,
- MATLAB/SIMULINK detailed models,
- Documented component selection,
- Lab testing to validate design,
- Rugged/dependable/durable design,
- Easy access to unit for troubleshooting,
- Monitoring and testing capability,
- Lessons learned (throughout thesis),
- Interface capable,
- Multiple mode configurations.

The SSCM design process began with component selection for the SSCM power section. Components were selected based on specifications provided by ESAC, available components, and theoretical calculations. Chapter III detailed the component selection process while Chapter IV documented the design of the closed-loop control algorithm. Each circuit was independently built and tested prior to final assembly. The dSPACE 1103 controller board and development software was utilized to test the control and PWM circuitry and proved to be an invaluable tool for design. A standard rack mount cabinet was used. The SSCM was constructed to be rugged, transportable, accessible, and possess the required space to efficiently house all required components. Digital pictures of each stage of the assembly were taken and recorded in Chapter V to assist in the construction and layout of future SSCM designs.

During construction, a detailed SIMULINK model of the SSCM was developed to test the control system for stability and capture the transient response. Once construction was completed, the SSCM was tested in the lab to ensure all protection circuitry functioned properly and that the SSCM met or exceeded all required system specifications.

B. FUTURE WORK

With DCZEDS offering enhanced survivability and improved automation, continued research in dc-dc converters is vital for the future of naval ship electrical systems. Many issues still must to be addressed in this design area. Possible areas for future research include:

- Electrical shielding of the SSCM to prevent switching noise interference,
- Soft-switching units to increase SSCM efficiency,
- The construction of a reduced-scale IPS at NPS to facilitate additional student thesis projects,
- Further and much more detailed use of dSPACE as a design tool,
- Construction of many SSCMs at different frequencies and power levels to compare efficiencies.

With IPS selected for DD-21, it is vital for research to continue in this area. DC-DC converters are an integral part of any DC distribution system and the Navy must continue with research in this area to ensure successful and reliable systems are delivered to the fleet.

APPENDIX A. DATA SHEETS

A. SEMIKRON RECTIFIER SKM 100 GB 124D IGBT

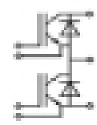
Absolute Maximum Ratings			
Symbol	Conditions [1]	Values	Units
V_{CES}		1200	V
V_{CGR}	R_{GE} = 20 kΩ	1200	V
I_C	T_{case} = 25/85 °C	150 / 100	A
I_{CM}	T_{case} = 25/85 °C; t_p = 1 ms	300 / 200	A
V_{GES}		± 20	V
P_{tot}	per IGBT, T_{case} = 25 °C	700	W
T_j, (T_{stg})		–40 ... + 150 (125)	°C
V_{isol}	AC, 1 min.	2 500	V
humidity	DIN 40040	Class F	
climate	DIN IEC 68 T.1	40/125/56	
Inverse Diode			
$I_F = -I_C$	T_{case} = 25/80 °C	95 / 65	A
$I_{FM} = -I_{CM}$	T_{case} = 25/80 °C; t_p = 1 ms	300 / 200	A
I_{FSM}	t_p = 10 ms; sin.; T_j = 150 °C	720	A
I^2t	t_p = 10 ms; T_j = 150 °C	2600	A^2s

Characteristics					
Symbol	Conditions [1]	min.	typ.	max.	Units
$V_{(BR)CES}$	V_{GE} = 0, I_C = 4 mA	≥ V_{CES}	–	–	V
$V_{GE(th)}$	$V_{GE} = V_{CE}$, I_C = 2 mA	4,5	5,5	6,5	V
I_{CES}	V_{GE} = 0, $V_{CE} = V_{CES}$; T_j = 25 °C	–	0,1	1,5	mA
	V_{GE} = 0, $V_{CE} = V_{CES}$; T_j = 125 °C	–	6	–	mA
I_{GES}	V_{GE} = 20 V, V_{CE} = 0	–	–	300	nA
V_{CEsat}	I_C = 75 A; V_{GE} = 15 V; T_j = 25 (125) °C	–	2,1(2,4)	2,45(2,85)	V
V_{CEsat}	I_C = 100 A; V_{GE} = 15 V; T_j = 25 (125) °C	–	2,5(3,0)	–	V
g_{fs}	V_{CE} = 20 V, I_C = 75 A	31	–	–	S
C_{CHC}	per IGBT	–	–	350	pF
C_{ies}	V_{GE} = 0; V_{CE} = 25 V; f = 1 MHz	–	5	6,6	nF
C_{oes}	V_{GE} = 0; V_{CE} = 25 V; f = 1 MHz	–	720	900	pF
C_{res}	V_{GE} = 0; V_{CE} = 25 V; f = 1 MHz	–	380	500	pF
L_{CE}		–	–	30	nH
$t_{d(on)}$	V_{CC} = 600 V; V_{GE} = –15 V / +15 V [3]; I_C = 75 A, ind. load; $R_{Gon} = R_{Goff}$ = 10 Ω; T_j = 125 °C	–	80	–	ns
t_r		–	45	–	ns
$t_{d(off)}$		–	430	–	ns
t_f		–	55	–	ns
E_{on} [4]		–	11	–	mWs
E_{off} [4]		–	9	–	mWs
Inverse Diode [5]					
$V_F = V_{EC}$	I_F = 75 A; V_{GE} = 0 V; T_j = 25 (125) °C	–	2,0(1,8)	2,5	V
$V_F = V_{EC}$	I_F = 100 A; V_{GE} = 0 V; T_j = 25 (125) °C	–	2,25(2,05)	–	V
V_{TO}	T_j = 125 °C	–	1,1	1,2	V
r_t	T_j = 125 °C	–	–	15	mΩ
I_{RRM}	I_F = 75 A; T_j = 125 °C [2]	–	42	–	A
Q_{rr}	I_F = 75 A; T_j = 125 °C [2]	–	9,1	–	µC
Thermal characteristics					
R_{thjc}	per IGBT	–	–	0,18	°C/W
R_{thjc}	per diode	–	–	0,50	°C/W
R_{thch}	per module	–	–	0,05	°C/W

SEMITRANS® M
Low Loss IGBT Modules

SKM 100 GB 124 D

SEMITRANS 2



GB

Features

- MOS input (voltage controlled)
- N channel, homogeneous Silicon structure (NPT- Non punch-through IGBT)
- Low loss high density chip
- Low tail current
- High short circuit capability, self limiting to 6 * I_{cnom}
- Latch-up free
- Fast & soft inverse CAL diodes [5]
- Isolated copper baseplate using DCB Direct Copper Bonding Technology without hard mould
- Large clearance (10 mm) and creepage distances (20 mm)

Typical Applications:
→ **B 6 – 121**
- Switching (not for linear use)

[1] T_{case} = 25 °C, unless otherwise specified
[2] $I_F = -I_C$, V_R = 600 V, $-di_F/dt$ = 800 A/µs, V_{GE} = 0 V
[3] Use V_{GEoff} = –5... –15 V
[4] See fig. 2 + 3; R_{Goff} = 10 Ω
[5] CAL = Controlled Axial Lifetime Technology

Cases and mech. data
→ **B 6 – 122**

 0898

SKM 100 GB 124 D

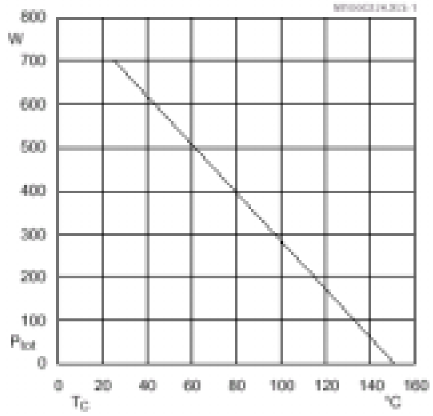


Fig. 1 Rated power dissipation $P_{tot} = f(T_C)$

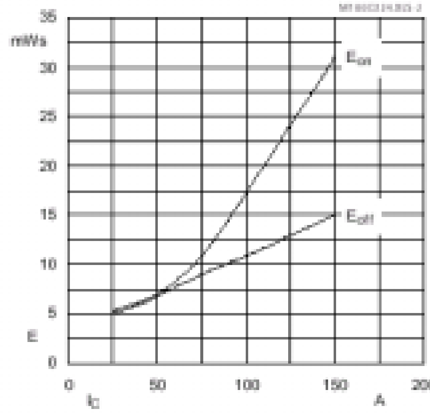


Fig. 2 Turn-on /-off energy = f (I_C)

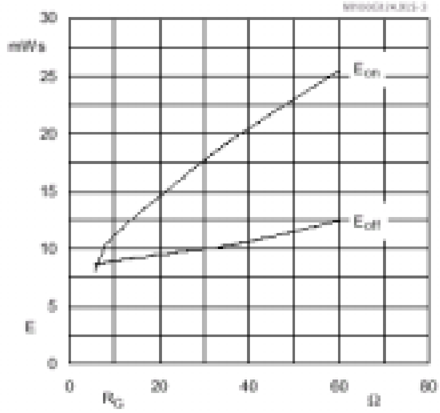


Fig. 3 Turn-on /-off energy = f (R_G)

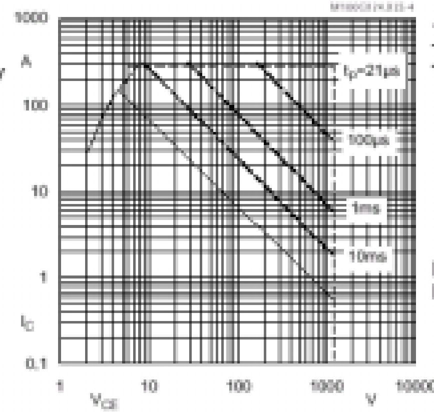


Fig. 4 Maximum safe operating area (SOA) $I_C = f(V_{CE})$

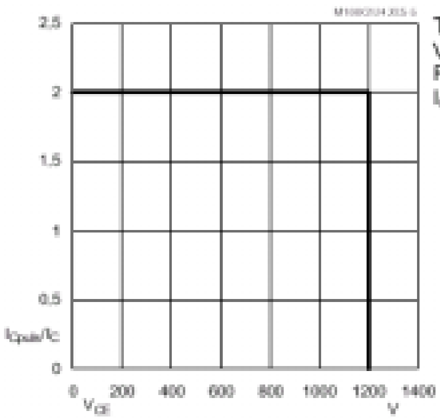


Fig. 5 Turn-off safe operating area (RBSOA)

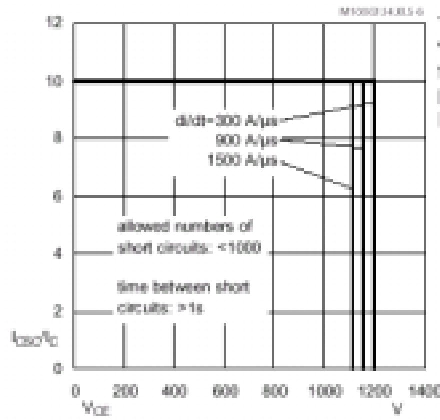


Fig. 6 Safe operating area at short circuit $I_C = f(V_{CE})$

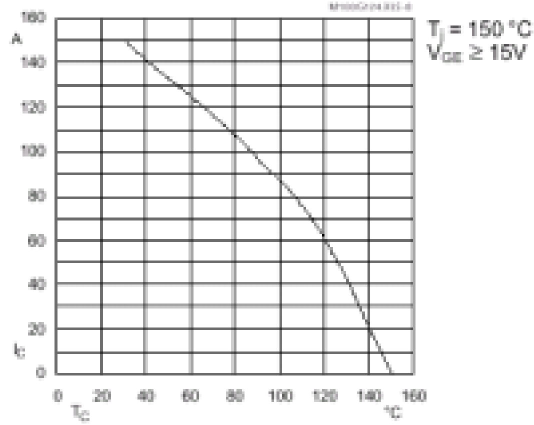


Fig. 8 Rated current vs. temperature $I_C = f(T_C)$

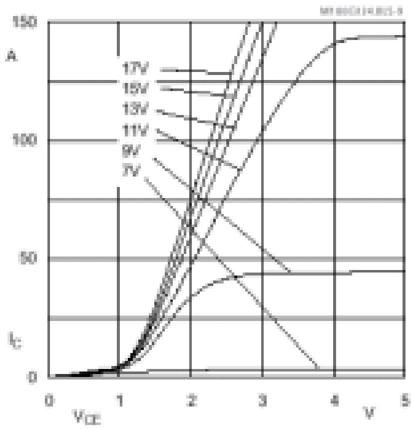


Fig. 9 Typ. output characteristic, t_p = 80 µs; 25 °C

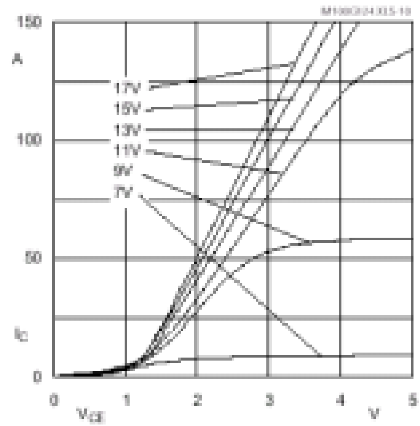


Fig. 10 Typ. output characteristic, t_p = 80 µs; 125 °C

$P_{cond(t)} = V_{CEsat(t)} \cdot I_{C(t)}$

$V_{CEsat(t)} = V_{CE(TO)(Tj)} + r_{CE(Tj)} \cdot I_{C(t)}$

$V_{CE(TO)(Tj)} \leq 1{,}3 + 0{,}0005\,(T_j - 25)$ [V]

typ.: $r_{CE(Tj)} = 0{,}0107 + 0{,}000033\,(T_j - 25)$ [Ω]

max.: $r_{CE(Tj)} = 0{,}0153 + 0{,}000047\,(T_j - 25)$ [Ω]

valid for $V_{GE} = +15\,^{+2}_{-1}$ [V]; $I_C > 0{,}3\,I_{Cnom}$

Fig. 11 Saturation characteristic (IGBT)
Calculation elements and equations

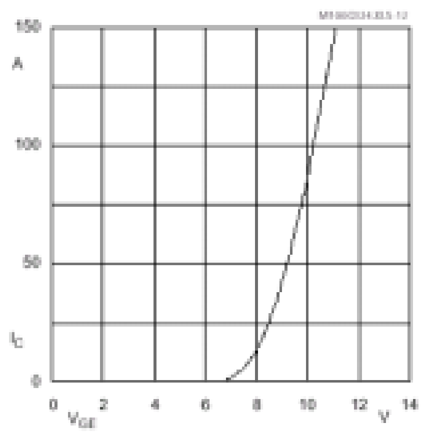


Fig. 12 Typ. transfer characteristic, t_p = 80 µs; V_{CE} = 20 V

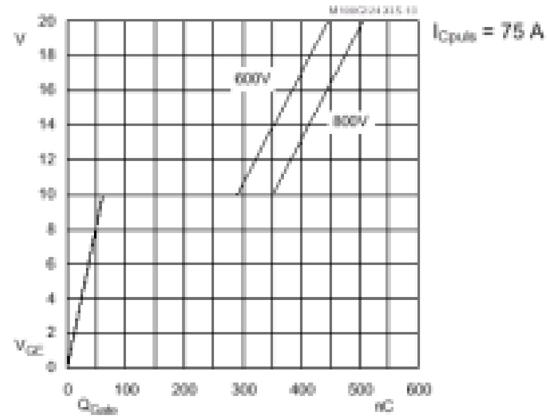


Fig. 13 Typ. gate charge characteristic

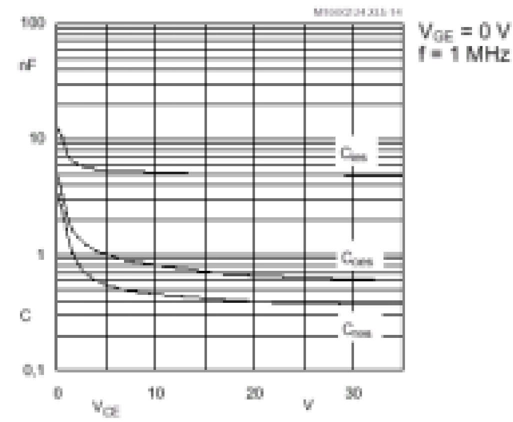


Fig. 14 Typ. capacitances vs.V_{CE}

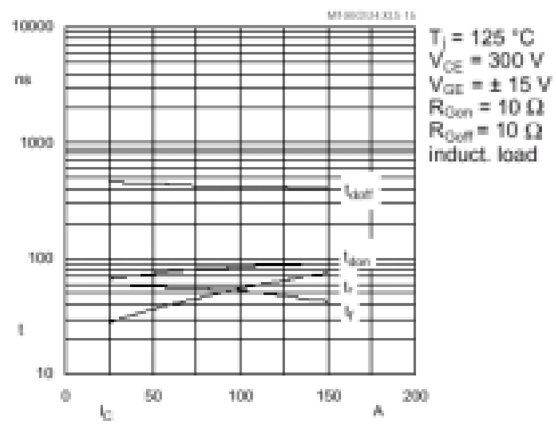


Fig. 15 Typ. switching times vs. I_C

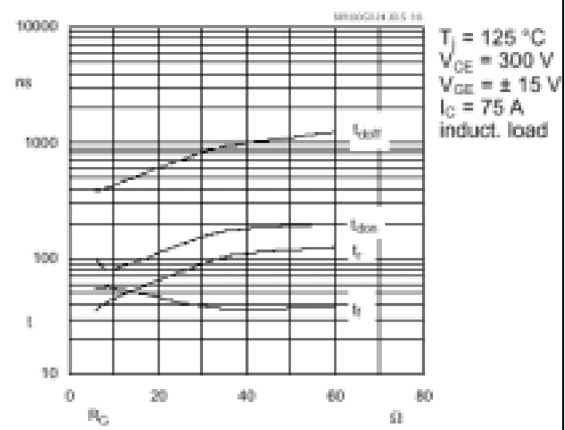


Fig. 16 Typ. switching times vs. gate resistor R_G

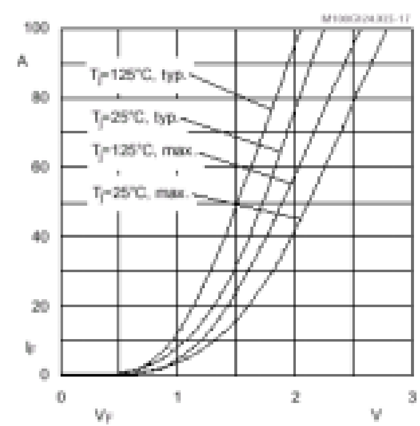


Fig. 17 Typ. CAL diode forward characteristic

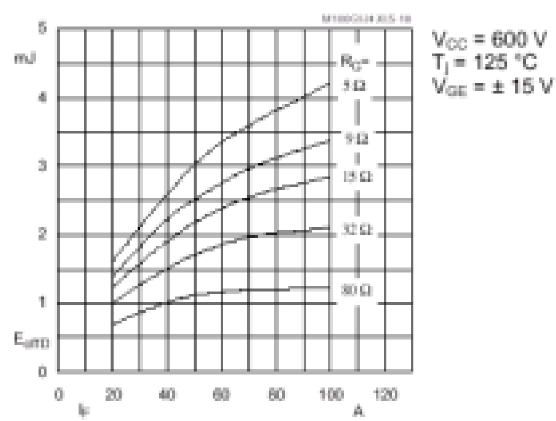


Fig. 18 Diode turn-off energy dissipation per pulse

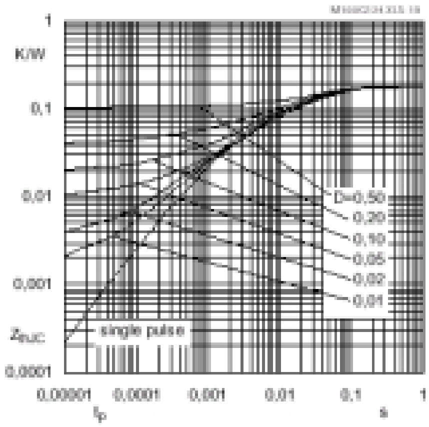


Fig. 19 Transient thermal impedance of IGBT
$Z_{thJC} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

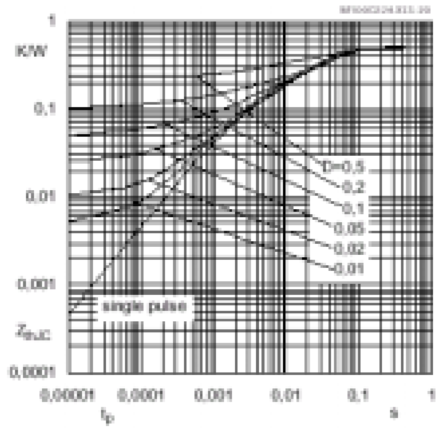


Fig. 20 Transient thermal impedance of inverse CAL diodes

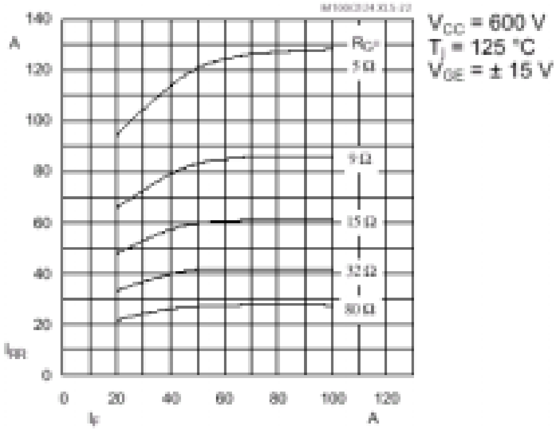


Fig. 22 Typ. CAL diode peak reverse recovery current $I_{RR} = f(I_F; R_G)$

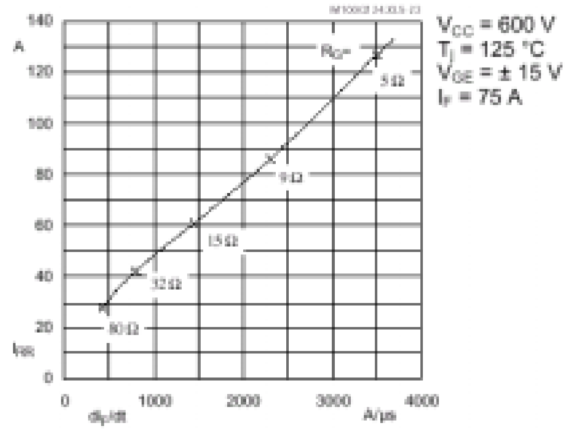


Fig. 23 Typ. CAL diode peak reverse recovery current $I_{RR} = f(di/dt)$

Typical Applications include

Switched mode power supplies
DC servo and robot drives
Inverters
DC choppers
AC motor speed control
UPS Uninterruptable power supplies
General power switching applications

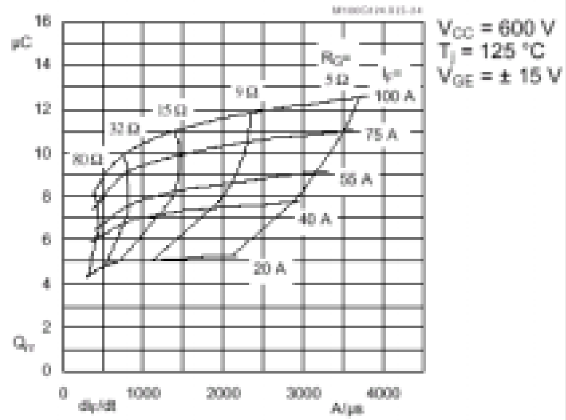


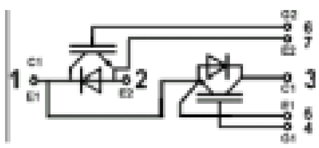
Fig. 24 Typ. CAL diode recovered charge

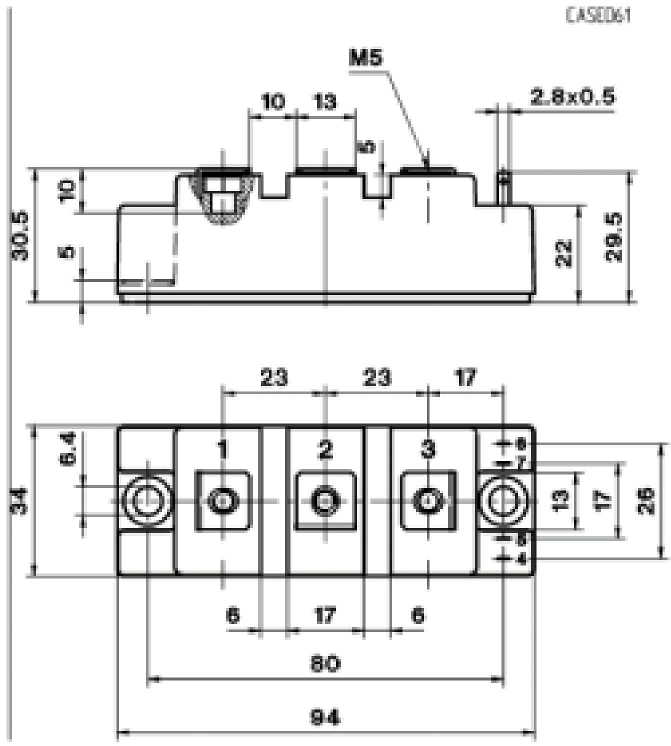
SKM 100 GB 124 D

SEMITRANS 2

Case D 61
UL Recognized
File no. E 63 532

SKM 100 GB 124 D





Dimensions in mm

Case outline and circuit diagram

Mechanical Data						
Symbol	**Conditions**		**Values**			**Units**
			min.	**typ.**	**max.**	
M_1	to heatsink, SI Units	(M6)	3	–	5	Nm
	to heatsink, US Units		27	–	44	lb.in.
M_2	for terminals, SI Units	(M5)	2,5	–	5	Nm
	for terminals, US Units		22	–	44	lb.in.
a			–	–	5x9,81	m/s^2
w			–	–	160	g

This is an electrostatic discharge sensitive device (ESDS). Please observe the international standard IEC 747-1, Chapter IX.

Eight devices are supplied in one SEMIBOX A without mounting hardware, which can be ordered separately under Ident No. 33321100 (for 10 SEMITRANS 2)

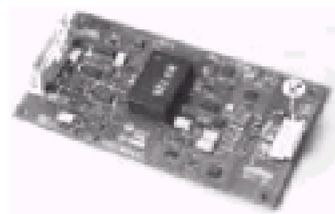
Larger packing units of 20 or 42 pieces are used if suitable

Accessories → B 6 – 4
SEMIBOX → C – 1.

B. SEMIKRON IGBT DRIVER BOARD

SEMIDRIVER®

High Power IGBT Driver
SKHI 10 [5)]
SKHI 10/17 [6)]



Absolute Maximum Ratings (Ta=25 °C)			
Symbol	**Term**	**Values**	**Unit**
V_S	Supply voltage primary	18	V
V_{iH}	Inputsignal voltage (HIGH) (for 15 V and 5 V input level)	VS + 0,3	V
$Iout_{PEAK}$	Output peak current	± 8	A
$Iout_{AVmax}$	Output average current (max.)	± 100	mA
V_{CE}	Collector-emitter voltage sense	1200[5)] / 1700[6)]	V
dv/dt	Rate of rise and fall of voltage (secondary to primary side)	75	kV/µs
$V_{isol\,IO}$	Isolation test volt. IN-OUT (1min.)	4000	V~
$R_{gon\,min}$	minimal R_{gon}	2,7	Ω
$R_{goff\,min}$	minimal R_{goff}	2,7	Ω
$Q_{out/pulse}$	charge per pulse	9,6	µC
T_{op}	Operating temperature	– 25 ... + 85	°C
T_{stg}	Storage temperature	– 25 ... + 85	°C

Electrical Characteristics (Ta=25 °C)					
Symbol	**Term**	**Values**			**Unit**
		min	**typ**	**max**	
V_S	Supply voltage primary	14,4	15,0	15,6	V
I_S	Supply current (max.)		0,3 [1)]		A
I_{SO}	Supply current primary side (no load)		90		mA
V_{iT+}	Input threshold voltage (HIGH) for				
	15 V input level	12,5			V
	for 5 V input level	2,4			V
V_{iT-}	Input threshold voltage (LOW) for				
	15 V input level			3,6	V
	for 5 V input level			0,50	V
$V_{G(on)}$	Turn-on output gate voltage		+ 15		V
$V_{G(off)}$	Turn-off output gate voltage		– 8		V
f	Maximum operating frequency		see fig. 15		
$td(on)_{IO}$	Input-output turn-on propagation time		1,4 [2)]		µs
$td(off)_{IO}$	Input-output turn-off propagation time		1,4 [2)]		µs
$t_{d(err)}$	Error input-output propagation time		1,0 [3)]		µs
V_{CEstat}	Reference voltage for V_{CE} monitoring		5,2 [5)] / 6,3 [6)]		V
R_{IN}	Input resistance		10		kΩ
R_{gon}	Internal gate resistor for ON signal		22 [4)]		Ω
R_{goff}	Internal gate resistor for OFF signal		22 [4)]		Ω
C_{ps}	Primary to secondary capacitance		12		pF

1) This current value is a function of the output load condition
2) Typical value
3) This value does not consider t_{ON} of IGBT and t_{MIN} adjusted by R_{CE} and C_{CE}
4) Matched to be used with IGBTs < 100 A; for higher currents, see table 2
5) With R_{CE} = 18 kΩ, C_{CE} = 330 pF; see fig. 6 (SKHI 10; for IGBT up to 1200 V)
6) With R_{CE} = 36 kΩ, C_{CE} = 470 pF; (SKHI 10/17; for IGBT up to 1700 V)

Features

- Single driver circuit for high power IGBTs
- SKHI 10 drives all SEMIKRON IGBTs with V_{CES} up to 1200 V (factory adjustment of V_{CES}-monitoring for 1200 V-IGBT)
- SKHI 10/17 drives all SEMIKRON IGBTs with V_{CE} up to 1700 V (factory adjustment of V_{CE}-monitoring for 1700 V-IGBT)
- CMOS/TTL (HCMOS) compatible input buffers
- Short circuit protection by V_{CE} monitoring
- Soft short circuit turn-off
- Isolation due to transformers (no opto couplers)
- Supply undervoltage monitoring (< 13 V)
- Error memory / output signal (LOW or HIGH logic)
- Internal isolated power supply

Typical Applications

- High frequency SMPS
- Braking choppers
- Asymmetrical bridges
- High power UPS

Block diagram SKHI10

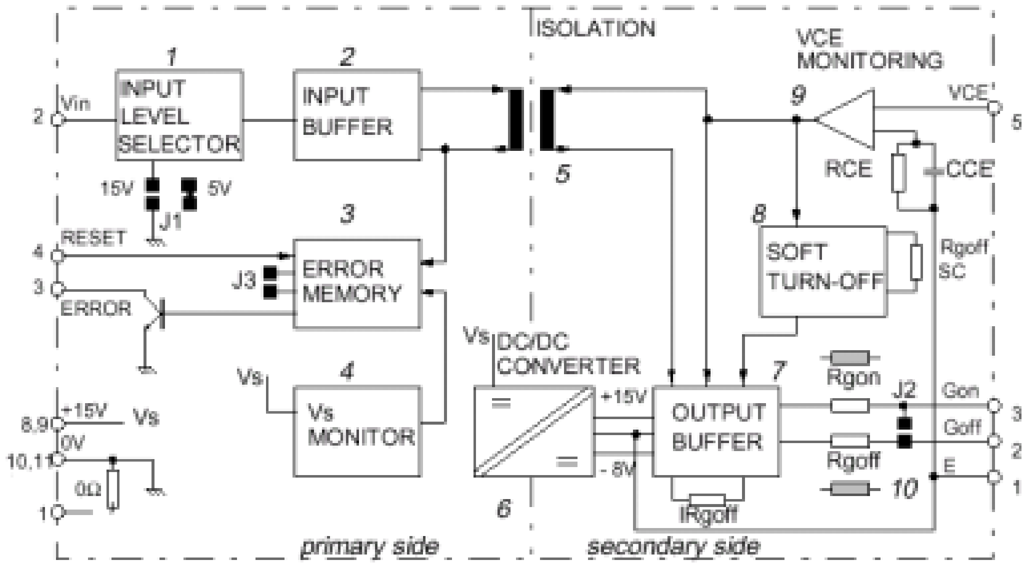
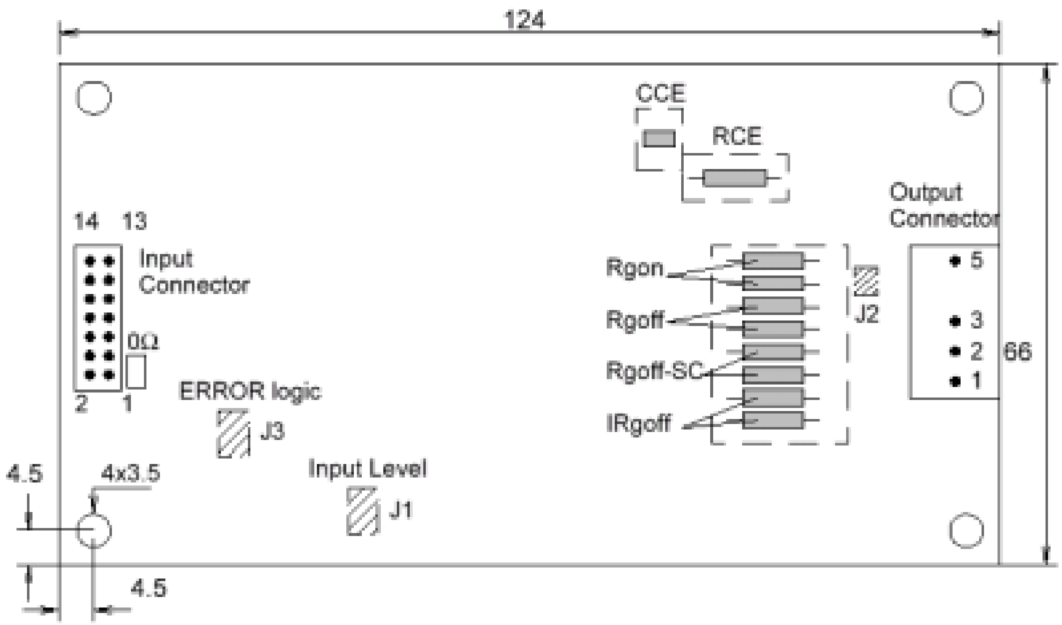


Fig.1 The numbers refer to the description on page 4, section B.



Input connector = 14 pin flat cable according to DIN 41651
Output connector = MOLEX 41791 Series (mates with 41695 crimp terminal housing and crimp terminals 7258)

Fig.2 Dimensions (in mm) and connections of the SKHI 10

SEMIDRIVER® SKHI 10
SEMIDRIVER® SKHI 10/17
High Power Single IGBT Driver

General

The intelligent single IGBT driver, SKHI10 respectively SKHI 10/17 is a standard driver for all power IGBTs on the market.
The high power output capability was designed to switch high current modules or several paralleled IGBTs even for high frequency applications. The output buffer has been improved to make it possible to switch up to 400A IGBT modules at frequencies up to 20kHz.
A new function has been added to the short circuit protection circuitry (Soft Turn Off), this automatically increases the IGBT turn off time and hence reduces the DC voltage overvoltage spikes, enabling the use of higher DC-bus voltages. This means an increase in the final output power.
An integrated DC/DC converter with high galvanic isolation (4 kV) ensures that the user is protected from the high voltage (secondary side).
The power supplies for the driver may be the same as used in the control board (0/+15V) without the requirement of isolation. All information that is transmitted between input and output uses ferrite transformers, resulting in high dv/dt immunity (75kV/μs).
The driver input stage is connected directly to the control board output and due to different control board operating voltages the SKHI10's input circuit includes a user voltage level selector (+15V or +5V).

In the following only the designation SKHI 10 is used. This is valid for both driver versions. If something is to be explained special to SKHI 10/17 it will be descriped by marking SKHI 10/17.

A. Features and Configuration of the Driver

A short description is given below. For detailed information, please refer to section B.

a) The SKHI10 has an INPUT LEVEL SELECTOR circuit which is adusted by J1 for two different levels. It is present for CMOS (15V) level, but can be changed by the user to HCMOS (5V) level by solder bridging the pads marked J1 together. For long input cables, we do not recommend the 5V level due to possible disturbances emitted by the power side.

b) The ERROR MEMORY blocks the transmission of all turn-on signals to the IGBT if either a short circuit or malfunction of V_S is detected, and sends a signal to the external control board through an open collector transistor.

c) With a FERRITE TRANSFORMER the information between primary and secondary may flow in both directions and high levels of dv/dt and isolation are obtained.

d) A high frequency DC/DC CONVERTER avoids the requirement of external isolated power supplies to obtain the necessary gate voltage. An isolated ferrite transformer in half-bridge configuration supplies the necessary power to the gate of the IGBT. With this feature, we can use the same power supply used in the external control circuit, even if we are using more than one SKHI10, e.g. in H-bridge configurations.

e) Short circuit protection is provided by measuring the collector-emitter voltage with a V_{CE} MONITORING circuit. An additional circuit detects the short circuit after a delay (determined by R_{CE},C_{CE}) and decreases the turn off speed (adjusted by R_{goff}-SC) of the IGBT. SOFT TURN-OFF under fault conditions is necessary as it reduces the voltage overshoot and allows for a faster turn off during normal operation.

f) The OUTPUT BUFFER is responsible for providing the correct current to the gate of the IGBT. If these signals do not have sufficient power, the IGBT will not switch properly, and additional losses or even the destruction of the IGBT may occur. According to the application (switching frequency and gate charge of the IGBT) the equivalent value of R_{gon} and the R_{goff} must be matched to the optimum value. This can be done by putting additional parallel resistors R_{gon}, R_{goff} with those already on the board. If only one IGBT is to be used, (instead of parallel connection) only one cable could be connected between driver and gate by soldering the two J2 areas together.

Fig.1 shows a simplified block diagram of the SKHI10 driver. Some preliminary remarks will help the understanding:

- Regulated +15V must be present between pins 8,9 (V_s) and 10,11 (⊥); an input signal (ON or OFF command to the IGBTs) from the control system is supplied to pin 2 (V_{in}) where HIGH=ON and LOW=OFF.
- Pin 5 (V_{CE}) at secondary side is normally connected to the collector of the IGBT to monitor V_{CE}, but for initial tests without connecting the IGBT it must be connected to pin 1 (E) to avoid ERROR signal and enable the output signals to be measured.
- The RESET input must be connected to 0V to enable the V_{in} signal. If it is left opened, the driver will be blocked.
- To monitor the error signal, a pull-up resistor must be provided between pin 3 (ERROR) and V_s.

B. Description of the Circuit Block Diagram (Fig. 1)

The circuit in Fig. 1 shows the input on the left and output on the right (primary/secondary).

1. Input level circuit

This circuit was designed to accept two different logic voltage levels. The standard level is +15V (factory adjusted) intended for noisy environments or when long connections (l > 50 cm) between the external control circuit and SKHI10 are used, where noise immunity must be considerate. For

lower power, and short connections between control and driver, the TTL-HCMOS level (+5V) can be selected by carefully soldering the small areas of J1 together, specially useful for signals coming from µP based controllers.

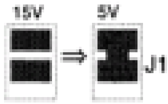


Fig.3 Selecting J1 for 5V level (TTL)

When connecting the SKHI10 to a control board using short connections no special attention needs to be taken (Fig. 4a).

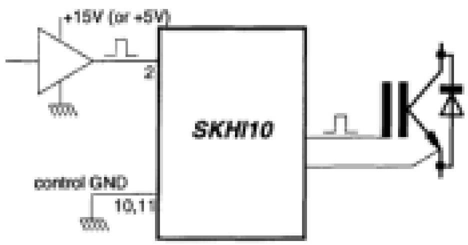


Fig.4a Connecting the SKHI10 with short cable

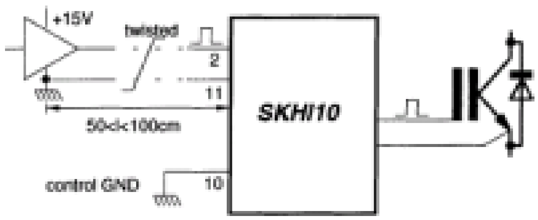


Fig.4b Connecting the SKHI10 with long cable

Otherwise, if the length is 50cm or more (we suggest to limit the cable length to about 1 meter), some care must be taken. The TTL level should be avoided and CMOS/15V is to be used instead; flat cable must have the pairs of conductors twisted or be shielded to reduce EMI/RFI susceptibility (Fig. 4b). If a shielded cable is used, it can be connected to pin 1. It is coupled to 0V through a resistor (O Ω).

As the input impedance of the INPUT LEVEL SELECTOR circuit is very high, an internal pull-down resistor keeps the IGBT in OFF state in case the Vin connection is interrupted or left non connected.

2. Input buffer

This circuit enables and amplifies the input signal Vin to be transferred to the pulse transformer when RESET (pin 4) is LOW and also prevents spurious signals being transmitted to the secondary side.

The following overview is showing the input threshold voltages

V_{IT+} (High)	min	typ	max
15 V	9,5 V	11,0 V	12,5 V
5 V	1,8 V	2,0 V	2,4 V

V_{IT-} (Low)	min	typ	max
15 V	3,6 V	4,2 V	4,8 V
5 V	0,50 V	0,65 V	0,80 V

3. Error memory and reset signal

The ERROR memory is triggered only by following events:
- short circuit of IGBTs
- V_S-undervoltage

In case of short circuit, the V_{CE} monitor sends a trigger signal (fault signal) through the impulse transformer to a FLIP-FLOP on the primary side giving the information to an open-collector transistor (pin 3), which may be connected to the external control circuit as ERROR message in HIGH logic (or LOW if J3 is short-circuited). If V_S power supply falls below 13V for more than 0,5ms, the same FLIP-FLOP is set and pin 3 is activated. For HIGH logic (default), an external R_C must be connected preferentially in the control main board. In this way the connection between main board and driver is also checked .
If low-logic version is used (J3 short-circuited), an internal pull-up resistor (internally connected to V_S) is provided, and the signal from more SKHI10s can be connected together to perform an wired-or-circuit.

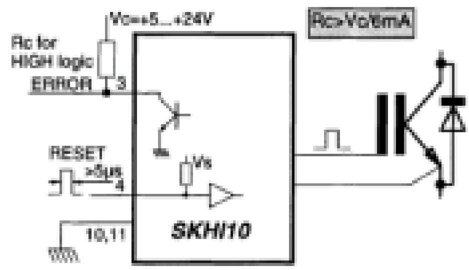


Fig.5 Driver status information ERROR, and RESET

The ERROR signal may be disabled either by RESET=HIGH (pin4) or by switching the power supply (V_S) off. The width of the RESET pulse must be more than 5µs, and in case of interrupted connection an internal pull-up resistor will act.

FAULT	RESET	ERROR [1]	V_{in}
no	0	0	enable
no	1	0	disable
yes	0	1	disable
yes	1	0	disable

1) default logic (HIGH); for LOW logic the signals are complementary

Table 1 ERROR signal truth table

The open-collector transistor (pin 3) may be connected through a pull-up resistor to an external (internal V_S for the "low-logic" version) voltage supply +5V...+24V, limiting the current to $I_{sink} \leq$ 6mA.

4. Power supply (Vs) monitor

The supply voltage V_S is monitored. If it falls below 13V an ERROR signal is generated and the turn-on pulses for the IGBT's gate are blocked.

5. Pulse transformer

It transmits the turn-on and turn-off signals to the IGBT. In the reverse direction the ERROR signal from the V_{CE} monitoring is transmitted via the same transformer. The isolation is 4 kV.

6. DC/DC converter

In the primary side of the converter, a half-bridge inverter transfers the necessary energy from Vs to the secondary of a ferrite transformer. In the secondary side, a full bridge and filters convert the high frequency signal coming from the primary to DC levels (+15V/- 8V) that are stabilised by a voltage regulator circuit.

7. Output buffer

The output buffer is supplied by the +15V/- 8V from the DC/DC converter. If the operation proceeds normally (no fault), the on- and off-signal is transmitted to the gate of an IGBT through R_{gon} and R_{goff}. The output stage has a MOSFET pair that is able to source/sink up to 8A peak current to/from the gate improving the turn-on/off time of the IGBT. Additionally, we can select I_{Rgoff} (see Fig. 2) either to discharge the gate capacitance with a voltage source (standard) or with a current source, specially design for the 1700V IGBT series (it speeds up the turn-off time of the IGBT). The present factory setting is voltage source (I_{Rgoff} = 0Ω). Using the current source I_{Rgoff}, R_{goff} must be 0 Ω.

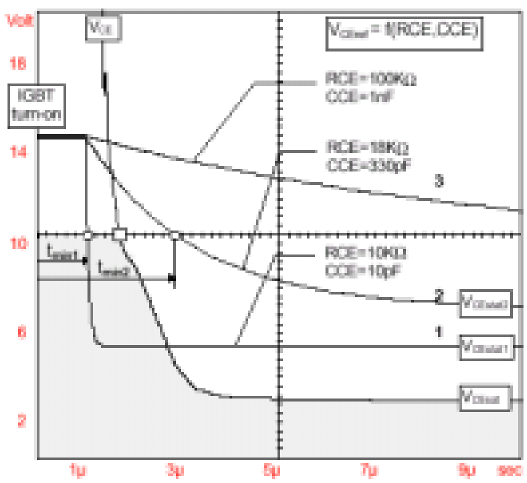


Fig.6 V_{CEref} waveform with parameters R_{CE}, C_{CE}

8. Soft turn-off

In case of short-circuit, a further circuit (SOFT TURN-OFF) increases the resistance in series with R_{goff} and turns-off the IGBT at a lower speed. This produces a smaller voltage spike (due LSTRAY x di/dt) above the DC link by reducing the di/dt value. Because in short-circuit conditions the Homogeneous IGBT's peak current increases up to 8 times the nominal current (up to 10 times with Epitaxial IGBT structures), and some stray inductance is ever present in power circuits, it must fall to zero in a longer time than at normal operation. This "soft turn-off time" can be reduced by connecting a parallel resistor R_{goff}-SC (see Fig. 2) with those already on the printed circuit board.

9. V_{CE} monitoring

This circuit is responsible for short-circuit sensing. Due to the direct measurement of V_{CEsat} on the IGBT's collector, it blocks the output buffer (through the soft turn-off circuit) in case of short-circuit and sends a signal to the ERROR memory on the primary side. The recognition of which V_{CE} level must be considered as a short circuit event, is adjusted by R_{CE} and C_{CE} (see Fig. 2), and it depends of the IGBT used. Typical values R_{CE} =18kΩ and C_{CE} =330 pF for SKHI 10 are delivered from factory (Fig. 6, curve 2). Using SKHI 10/17 the driver will be delivered with R_{CE} = 36 kΩ and C_{CE} = 470 pF from factory.

The V_{CEref} is not static but a dynamic reference which has an exponential shape starting at about 15V and decreases to V_{CEstat} (5V ≤ V_{CEstat} ≤ 10V determinated by R_{CE}), with a time constant τ (0,5 µs ≤ τ ≤ 1ms controlled by C_{CE}). The V_{CEstat} must be adjusted to remain above V_{CEsat} in normal operation (the IGBT is already in full saturation).

To avoid a false failure indication when the IGBT just starts to conduct (V_{CEsat} value is still too high) some decay time must be provided for the V_{CEref}. As the V_{CE} signal is internally limited at 10V, the decay time of V_{CEref} must reach this level after V_{CE} or a failure indication will occur (see Fig.6, curve 1). A t_{min} is defined as function of V_{CEstat} and τ to find out the best choice for R_{CE} and V_{CE} (see Fig.6, curve 2). The time the IGBT come to the 10V (represented by a "□" in Fig. 6) depends on the IGBT itself and R_{gon} used.

The R_{CE} and C_{CE} values can be found from Fig. 7 by taking the V_{CEstat} and t_{min} as input values with following remarks:

- R_{CE} > 10KΩ
- C_{CE} < 2,7nF

Attention!: If this function is not used, for example during the experimental phase, the V_{CE} MONITORING must be connected with the EMITTER output to avoid possible fault indication and consequent gate signal blocking.

10. R_{gon}, R_{goff}

These two resistors are responsible for the switching speed of each IGBT. As an IGBT has input capacitance (varying during the switching time) which must be charged and discharged, both resistors will dictate what time must be taken to do this. The final value of resistance is difficult to predict, because it depends on many parameters, as follows:

- DC-link voltage
- stray inductance of the circuit
- switching frequency
- type of IGBT

C. Operating Procedure

1. One IGBT connection

To realize the correct switching and short-circuit monitoring of one IGBT some additional external components must be used (Fig.8).

The driver is delivered with four R_g resistors (43Ω). This value can be reduced to use the driver with bigger modules or higher frequencies/lower voltages, by putting additional resistors in parallel to the existing ones.

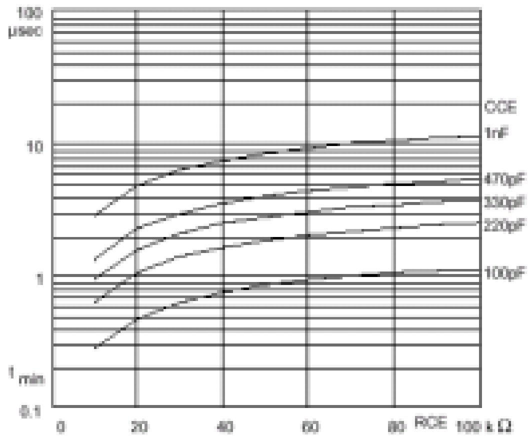


Fig.7a t_{min} as function of R_{CE} and C_{CE}

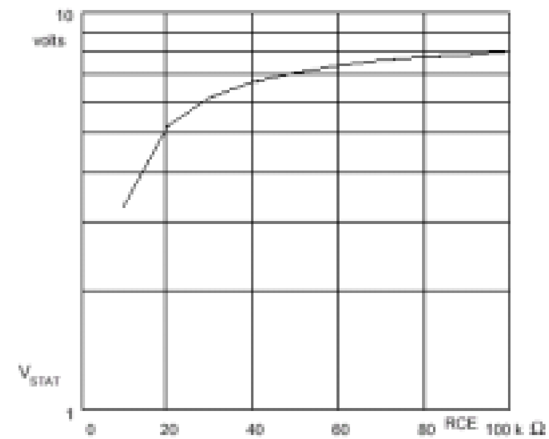


Fig. 7b V_{CEstat} as function of R_{CE}

The outputs G_{on} and G_{off} were previewed to connect the driver with more than one IGBT (paralleling). In that case we need both signals ON/OFF separately to connect additional external resistors R_{gon} and R_{goff} for each IGBT. If only one IGBT is to be used, we suggest to connect both points together through J2 (see Fig. 1 and 2). This can be done by soldering the two small pads together, which saves one external connection.

Typical component values: *)

SK-IGBT-Module	R_{Gon} Ω	R_{Goff} Ω	C_{CE} pF	R_{CE} kΩ	I_{Rgoff} Ω
SKM 75GAL123D	22	22	330	18	0
SKM 100GAL(R)123D	15	15	330	18	0
SKM 150GAL(R)123D	12	12	330	18	0
SKM 200GA(L/R)123D	10	10	330	18	0
SKM 300GA(L/R)123D	8,2	8,2	330	18	0
SKM 400GA123D	6,8	6,8	330	18	0
SKM 500GA123D	5,6	5,6	330	18	0

Table 2a 1200V IGBT@ DC-link< 700V

SK-IGBT-Module	R_{Gon} Ω	R_{Goff} Ω	C_{CE} pF	R_{CE} kΩ	I_{Rgoff} Ω
SKM 200GAL173D	8,2	8,2	470	36	0
SKM 300GA173D	6,8	6,8	470	36	0
SKM 400GA173	5,6	5,6	470	36	0

Table 2b 1700V IGBT@ DC-link< 1000V

*) Only starting values, for final optimization.

The adjustment of R_{goffSC} (factory adjusted R_{goffSC} = 22 Ω) should be done observing the overvoltages at the module in case of short circuit. When having a low inductive DC-link the module can be switched off faster.

The values shown should be considered as standard values for a mechanical/electrical assembly, with acceptable stray inductance level, using only one IGBT per SKHI10 driver. The final optimized value can be found only by measuring.

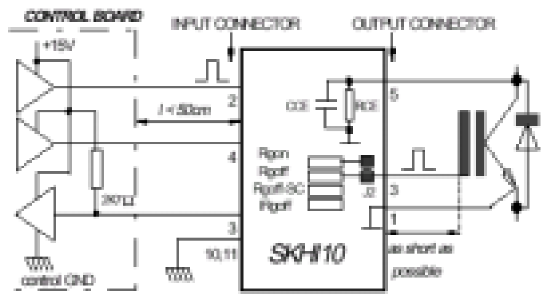


Fig. 8 Preferred standard circuit

2. Paralleling IGBTs

The parallel connection is recommended only by using IGBTs with homogeneous structure (IGHT), that have a positive temperature coefficient resulting in a perfect current sharing without any external auxiliary element. After all some care must be considered to reach an optimized circuit and to obtain the total performance of the IGBT (Fig. 9). The IGBTs must have independent values of R_{gon} and R_{goff}. An auxiliary emitter resistor R_e as well as an auxiliary collector resistor R_c must also be used.

The external resistors R_{gonx}, R_{goffx}, R_{ex} and R_{cx} should be mounted on an additional circuit board near the paralleled modules, and the R_{gon}/R_{goff} on the driver should be changed to zero ohms.
The R_{ex} assumes a value of 0,5Ω and its function is to compensate the wiring resistance in the auxiliary emitters what could make the emitter voltage against ground unbalanced.
The R_{cx} assumes a value of 47 Ω and its function is to create an average value of V_{CEsat} in case of short circuit for V_{CE}

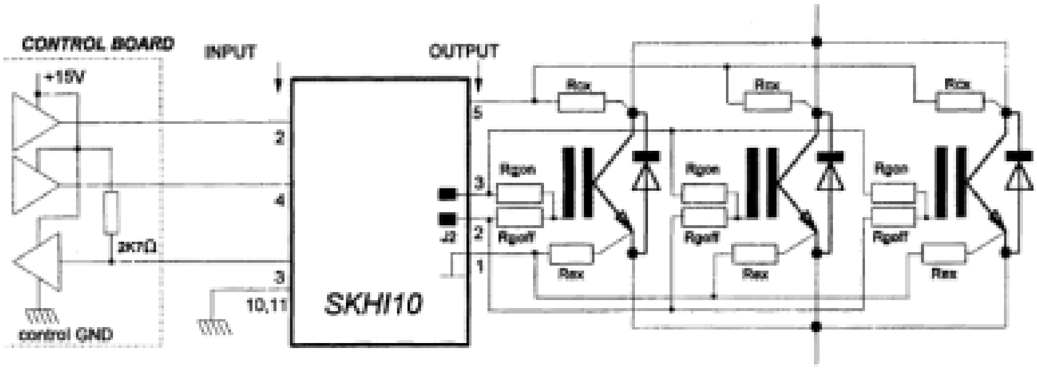


Fig.9 Preferred circuit for paralleled IGBTs

monitoring.
The mechanical assembly of the power circuit must be symmetrical and low inductive.
The maximum recommended gate charge is 9,6μC.
See also Fig.14.

D. Signal Waveforms

The following signal waveforms were measured under the conditions below:

- V_S = 15V
- T_{amb} = 25°C
- load = SKM150GAL161D
- R_{CE} = 18kΩ
- C_{CE} = 330pF
- U_{DC} = 1200V
- I_C = 100A

All results are typical values if not otherwise specified.

The limit frequency of SKHI10 depends on the gate charge connected in its output pins.
If small IGBT modules are used, the frequency could theo-

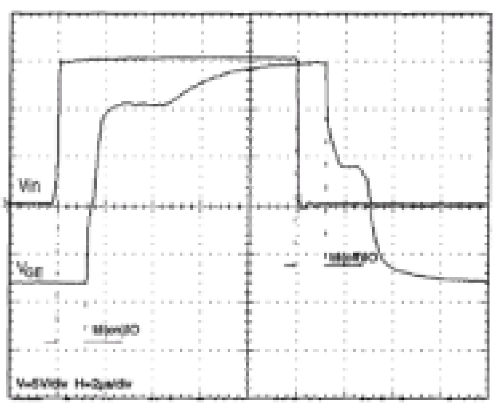


Fig.10 Input and output voltage propagation time

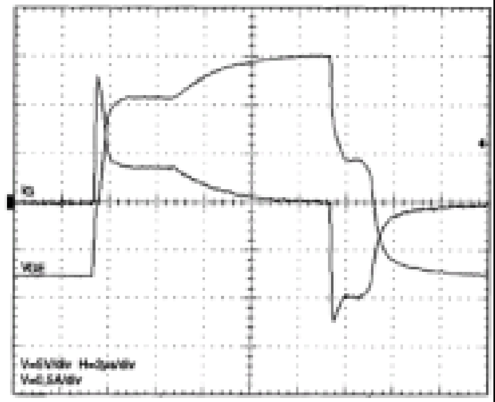


Fig.11 Output voltage (V_{GE}) and output current (I_G)

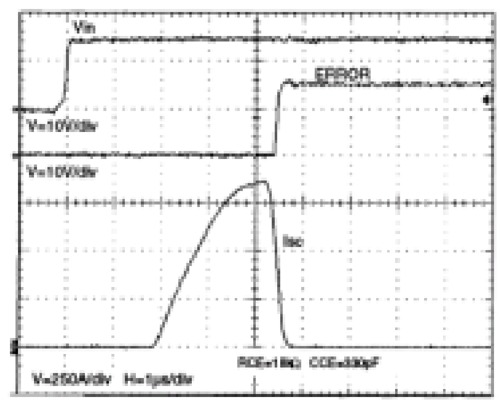


Fig.12 Short-circuit and ERROR propagation time worst-case (V_{in} with SC already present)

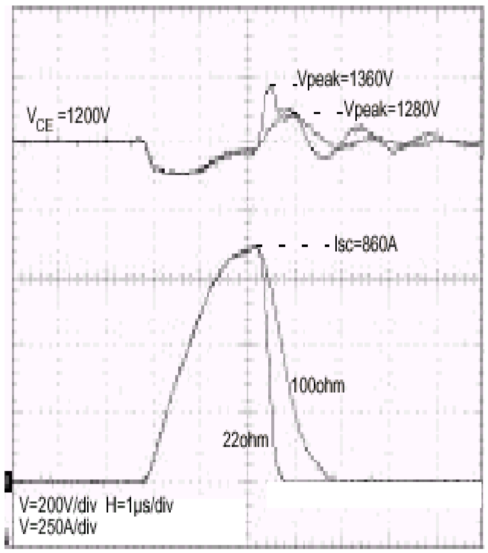


Fig.13 Effect of R_{goff}-SC in short - circuit

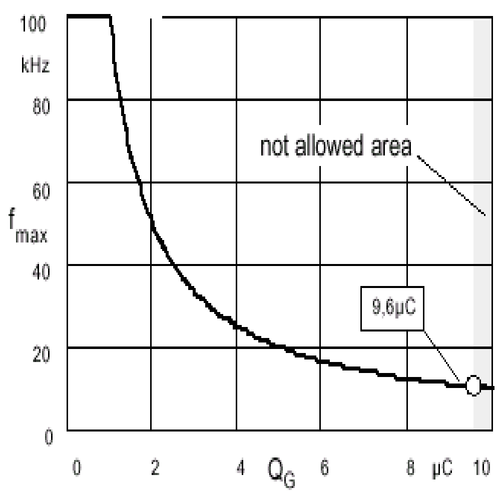


Fig.14 Maximum operating frequency x gate charge

retically reach 100kHz. For bigger modules or even paralleled modules, the maximum frequency must be determinate (Fig. 14). Q_G is the total equivalent gate charge connected to the output of the driver. The maximum allowed value is limited (9,6µC), and depends on the output internal capacitance connected to the power supply (energy storage capacitance).

E. Application / Handling

1. The CMOS inputs of the driver are extremely sensitive to overvoltage. Voltages higher than (V_S + 0,3 V) or under - 0,3 V may destroy these inputs.

Therefore the following safety requirements are to be observed:

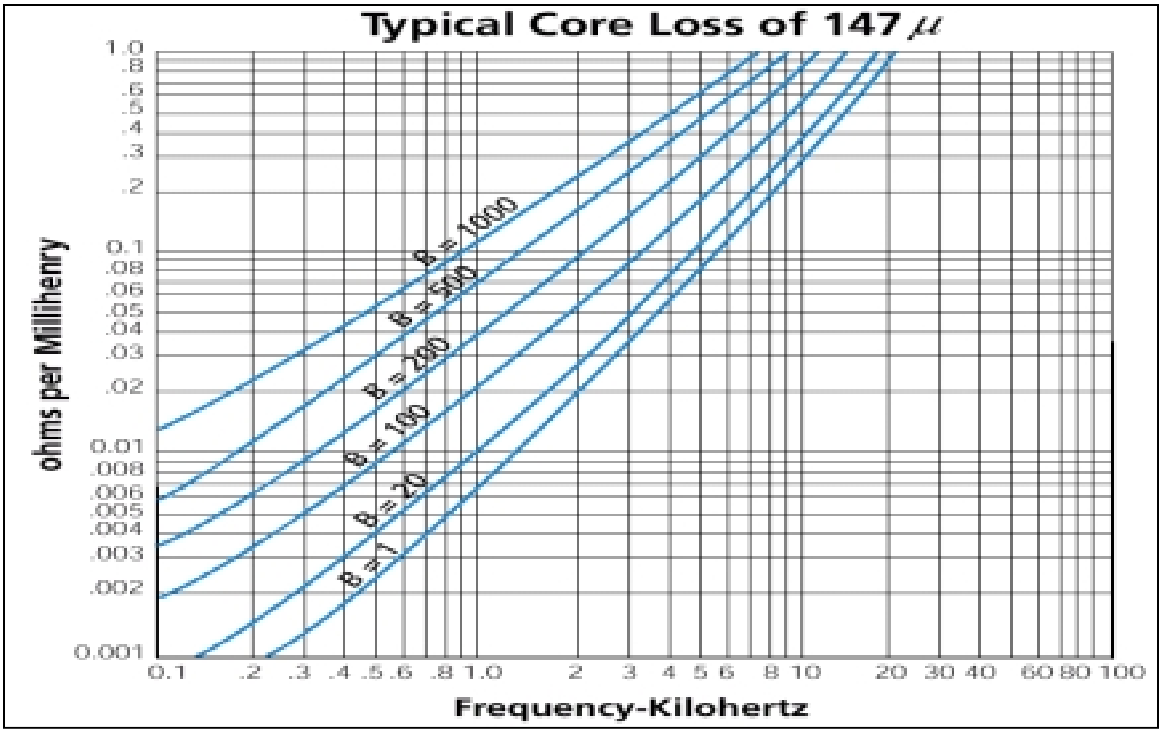
- To make sure that the control signals do not comprise overvoltages exceeding the above values.
- Protection against static discharges during handling. As long as the hybrid driver is not completely assembled the input terminals must be short circuited. Persons working with CMOS devices should wear a grounded bracelet. Any floor coverings must not be chargeable. For transportation the input terminals must be short circuited using, for example, conductive rubber. Places of work must be grounded. The same foam requirements apply to the IGBTs.

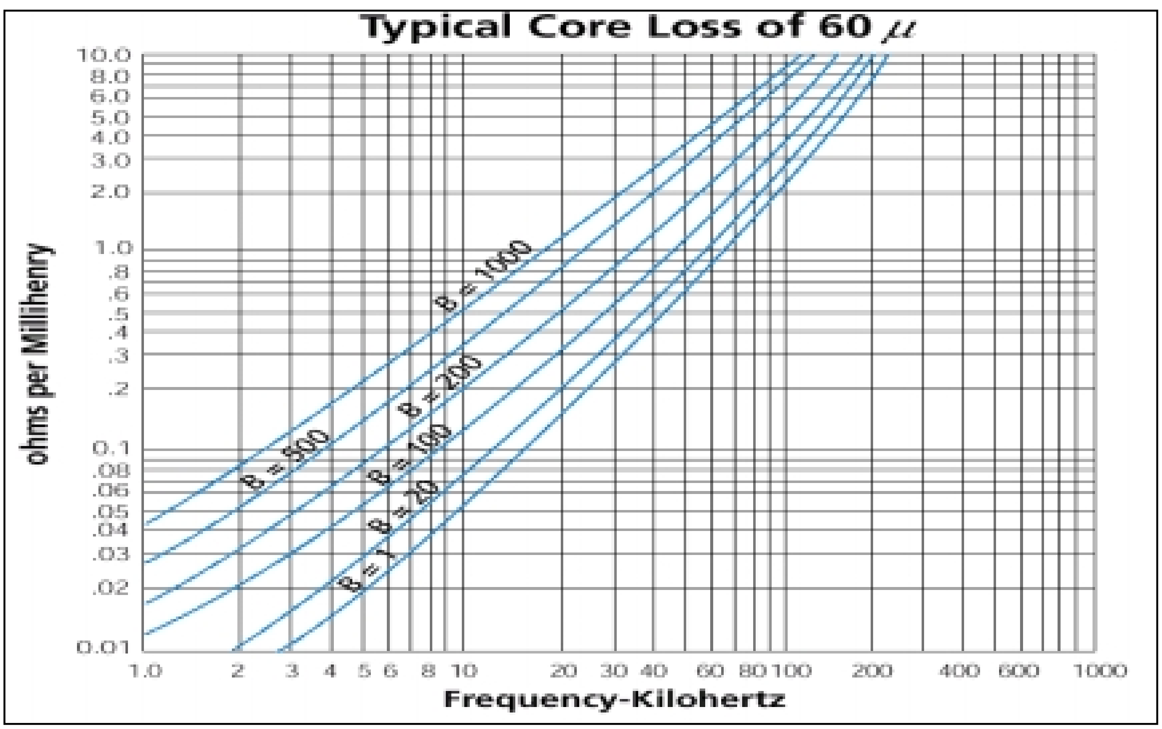
2. The connecting leads between the driver and the power module must be as short as possible, and should be twisted.
3. Any parasitic inductance should be minimized. Overvoltages may be damped by C or RCD snubber networks between the main terminals [3] = C1 (+) and [2] = E2 (-) of the power module.
4. When first operating a newly developed circuit, low collector voltage and load current should be used in the beginning. These values should be increased gradually, observing the turn-off behavior of the free-wheeling diodes and the turn-off voltage spikes across the IGBT by means of an oscilloscope. Also the case temperature of the power module should be monitored. When the circuit works correctly, short circuit tests can be made, starting again with low collector voltage.
5. It is important to feed any ERROR back to the control circuit to switch the equipment off immediately in such events. Repeated turn-on of the IGBT into a short circuit, with a frequency of several kHz, may destroy the device.

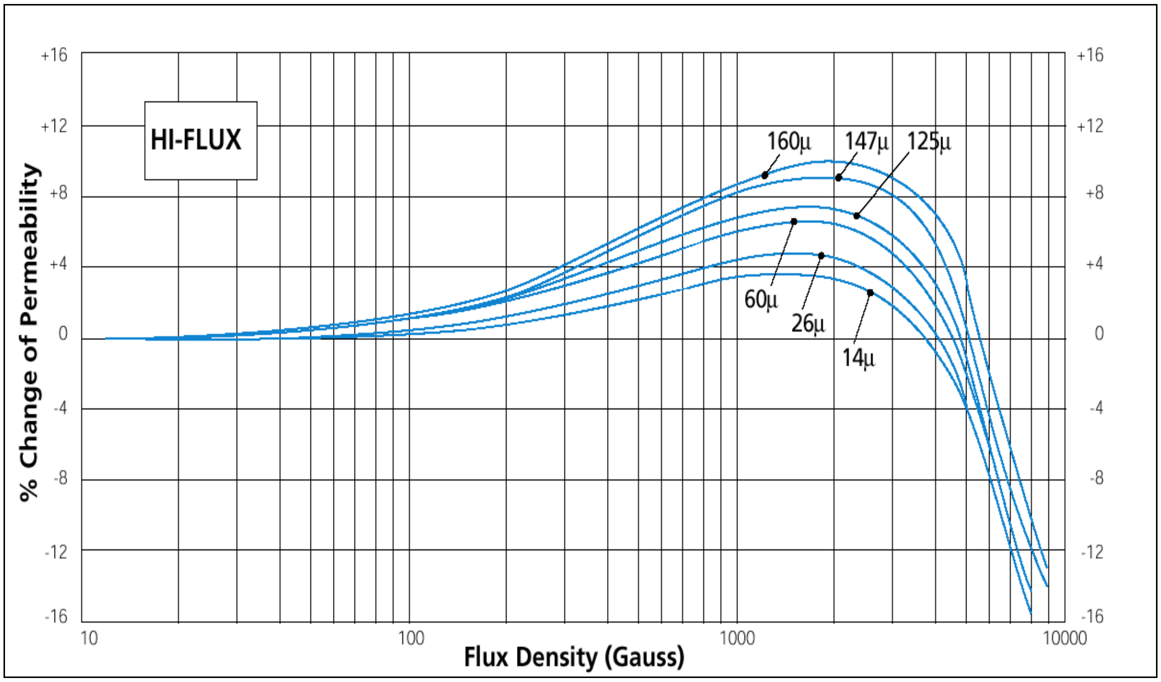
For further details ask SEMIKRON

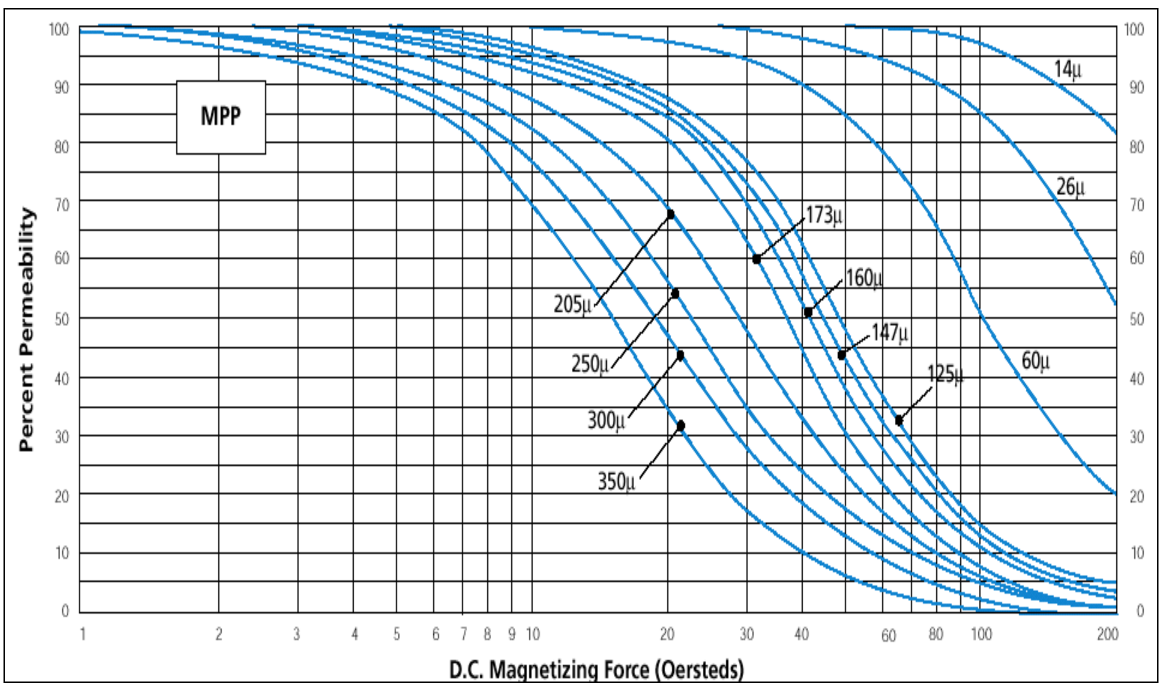
Nr.11224040

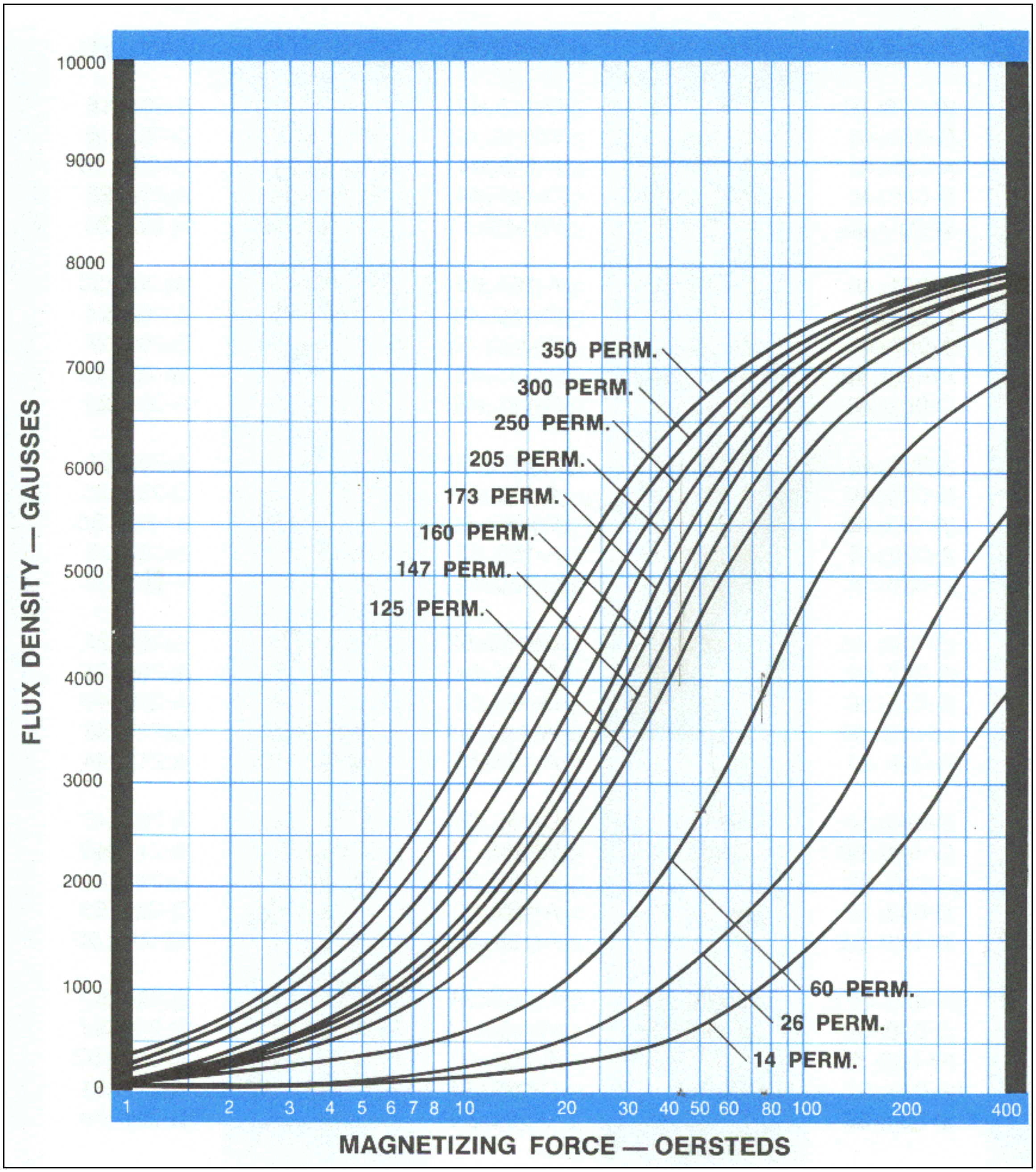
C. ARNOLD PC-104 MPP CORES





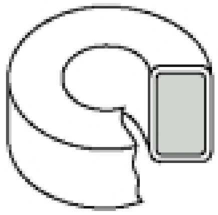

HI-FLUX
% Change of Permeability
Flux Density (Gauss)
+16
+12
+8
+4
0
-4
-8
-12
-16
10
100
1000
10000
160µ
147µ
125µ
60µ
26µ
14µ


MPP
Percent Permeability
D.C. Magnetizing Force (Oersteds)
100
90
80
70
60
50
40
30
20
10
0
1
2
3
4
5
6
7
8
9
10
20
30
40
60
80
100
200
14µ
26µ
60µ
125µ
147µ
160µ
173µ
205µ
250µ
300µ
350µ


10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
FLUX DENSITY — GAUSSES
350 PERM.
300 PERM.
250 PERM.
205 PERM.
173 PERM.
160 PERM.
147 PERM.
125 PERM.
60 PERM.
26 PERM.
14 PERM.
1
2
3
4
5
6
7
8
10
20
30
40
50
60
80
100
200
400
MAGNETIZING FORCE — OERSTEDS

o.d. 4.000

i.d. 2.250/ht. 0.650



CORNERS:

0.125 Approx. Radius (Typical)

Dimensions

	Outside Diameter	Inside Diameter	Height
Before Coating Nominal	4.000 in 101.60 mm	2.250 in 57.15 mm	0.650 in 16.51 mm
After Coating (Blue Epoxy)	4.050 in Max. 102.87 mm Max.	2.195 in Min. 55.75 mm Min.	0.700 in Max. 17.78 mm Max.

Physical Specifications

Effective Cross Sectional Area of Magnetic Path, A_e (Reference)	Effective Magnetic Path Length, l_e (Reference)	Effective Core Volume, V_e (Reference)	Minimum Window Area (Reference)	Approximate Weight of Finished 125µ MPP Core	Approximate Mean Length of Turn for Full Winding (Half of I.D. Remaining)
0.5460 in² 3.5226 cm²	9.555 in 24.271 cm	5.217 in³ 85.495 cm³	3.784 in² 24.413 cm² 4,818,025 cmil	1.61 lbs 730 g	3.29 in 8.35 cm

Electrical Specifications

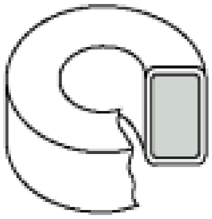
Nominal Permeability	Inductance Factor, mH +/- 8% for 1000 turns	Approximate Ratio of DC Resistance to Inductance for Full Winding (Half of I.D. Remaining), Ω/mH	Part Numbers		
			Molypermalloy	HI-FLUX	SUPER-MSS
14µ	25.6	0.049	A-658026-2	HF-400014-2	—
26µ	47.4	0.027	A-659047-2	HF-400026-2	MS-400026-2
60µ	112	0.011	A-125112-2	HF-400060-2	MS-400060-2
75µ	137	0.0092	—	—	MS-400075-2
90µ	164	0.0076	—	—	MS-400090-2
125µ	228	0.0055	A-542228-2	HF-400125-2	MS-400125-2
147µ	268	0.0047	A-157268-2	HF-400147-2	—
160µ	292	0.0043	A-660292-2	HF-400160-2	—
173µ	316	0.0040	A-184316-2	—	—
205µ	374	0.0034	A-220374-2	—	—

Heavy Film Magnet Wire Winding Data (Approximate)

AWG	Full Winding (Half of I.D. Remaining)		Single Layer Winding		
	Turns	R_{dc} Ω	Turns	R_{dc} Ω	l_w ft.
10	—	—	56	0.0158	15.8
11	—	—	63	0.0222	17.6
12	366	0.1678	70	0.0311	19.6
13	457	0.262	79	0.0436	21.8
14	573	0.410	88	0.0608	24.1
15	716	0.641	99	0.0854	26.9
16	896	1.008	111	0.120	29.9
17	1116	1.569	124	0.168	33.3
18	1396	2.47	139	0.236	37.0
19	1740	3.85	156	0.332	41.3
20	2166	6.01	174	0.464	45.8
21	2698	9.40	195	0.653	51.1
22	3380	14.88	218	0.924	57.0
23	4183	25.0	242	1.28	63.2
24	5215	36.1	271	1.81	70.3
25	6483	56.5	303	2.54	78.5
26	8094	89.2	338	3.59	87.5
27	10004	137.9	376	4.99	96.9

o.d. 5.218

i.d. 3.094/ht. 0.800



CORNERS:

0.125 Approx. Radius (Typical)

Dimensions

	Outside Diameter	Inside Diameter	Height
Before Coating Nominal	5.218 in 132.54 mm	3.094 in 78.59 mm	0.800 in 20.32 mm
After Coating (Blue Epoxy)	5.274 in Max. 133.96 mm Max.	3.033 in Min. 77.04 mm Min.	0.855 in Max. 21.72 mm Max.

Physical Specifications

Effective Cross Sectional Area of Magnetic Path, A_e (Reference)	Effective Magnetic Path Length, l_e (Reference)	Effective Core Volume, V_e (Reference)	Minimum Window Area (Reference)	Approximate Weight of Finished 125µ MPP Core	Approximate Mean Length of Turn for Full Winding (Half of I.D. Remaining)
0.8288 in² 5.3471 cm²	12.767 in 33.12 cm	10.58 in³ 173.40 cm³	7.225 in² 46.612 cm² 9,199,089 cmil	3.19 lbs 1450 g	3.97 in 10.09 cm

Electrical Specifications

Nominal Permeability	Inductance Factor, mH +/- 8% for 1000 turns	Approximate Ratio of DC Resistance to Inductance for Full Winding (Half of I.D. Remaining), Ω/mH	Part Numbers		
			Molypermalloy	HI-FLUX	SUPER-MSS
14µ	26	0.031	A-430026-2	HF-520014-2	—
26µ	54	0.015	A-129054-2	HF-520026-2	MS-520026-2
60µ	124	0.0064	A-128124-2	HF-520060-2	MS-520060-2
75µ	155	0.0052	—	—	MS-520075-2
90µ	187	0.0043	—	—	MS-520090-2
125µ	259	0.0031	A-127259-2	HF-520125-2	MS-520125-2
147µ	304	0.0026	A-158304-2	HF-520147-2	—
160µ	332	0.0024	A-661332-2	HF-520160-2	—
173µ	358	0.0022	A-185358-2	—	—
205µ	425	0.0019	A-221425-2	—	—

Heavy Film Magnet Wire Winding Data (Approximate)

AWG	Full Winding (Half of I.D. Remaining)		Single Layer Winding		
	Turns	R_{dc} Ω	Turns	R_{dc} Ω	L_w ft.
10	—	—	78	0.0266	26.6
11	—	—	88	0.0374	29.6
12	695	0.382	98	0.0524	33.0
13	869	0.598	110	0.0735	36.7
14	1088	0.937	123	0.103	40.6
15	1360	1.467	138	0.144	45.3
16	1702	2.31	155	0.203	50.5
17	2121	3.60	173	0.284	56.2
18	2652	5.65	193	0.400	62.6
19	3307	8.84	216	0.562	69.8
20	4116	13.80	241	0.786	77.6
21	5127	21.6	270	1.11	86.5
22	6421	34.2	302	1.56	96.5
23	7947	52.9	336	2.17	107
24	9908	83.2	375	3.06	119
25	12318	130.1	420	4.31	133

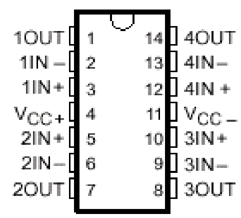
D. LF347 QUAD OPERATIONAL AMPLIFIERS

LF347, LF347B JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

SLOS013B – MARCH 1987 – REVISED AUGUST 1994

- **Low Input Bias Current . . . 50 pA Typ**
- **Low Input Noise Current 0.01 pA/$\sqrt{Hz}$ Typ**
- **Low Total Harmonic Distortion**
- **Low Supply Current . . . 8 mA Typ**
- **Gain Bandwidth . . . 3 MHz Typ**
- **High Slew Rate . . . 13 V/µs Typ**
- **Pin Compatible With the LM348**

D OR N PACKAGE
(TOP VIEW)



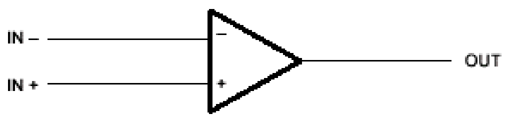
description

These devices are low-cost, high-speed, JFET-input operational amplifiers. They require low supply current yet maintain a large gain-bandwidth product and a fast slew rate. In addition, their matched high-voltage JFET inputs provide very low input bias and offset current.

The LF347 and LF347B can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF347 and LF347B are characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	10 mV	LF347D	LF347N
	5 mV	LF347BD	LF347BN

The D packages are available taped and reeled. Add R suffix to the device type (e.g., LF347DR).

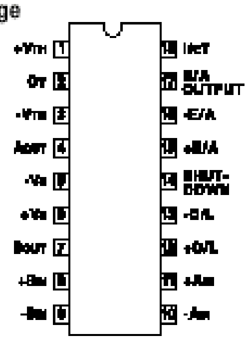
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} . . . . . 18 V
Supply voltage, V_{CC-} . . . . . –18 V
Differential input voltage, V_{ID} . . . . . ±30 V
Input voltage, V_I (see Note 1) . . . . . ±15 V
Duration of output short circuit . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

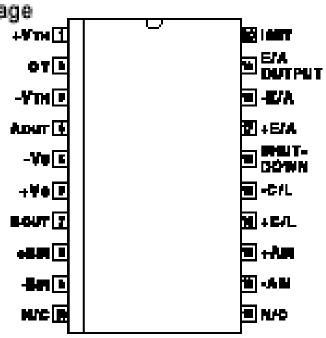
NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

CONNECTION DIAGRAM

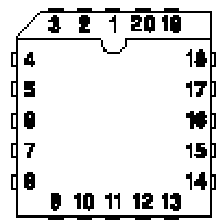
DIL-18 (TOP VIEW)
J or N Package



SOIC-20 (TOP VIEW)
DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
$+V_{TH}$	1
C_T	2
$-V_{TH}$	3
A_{OUT}	4
$-V_S$	5
N/C	6
$+V_S$	7
B_{OUT}	8
$+B_{IN}$	9
$-B_{IN}$	10
$-A_{IN}$	11
$+A_{IN}$	12
+C/L	13
-C/L	14
SHUTDOWN	15
N/C	16
+E/A	17
-E/A	18
E/A OUTPUT	19
I_{SET}	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637; $+V_S$ = +15V, $-V_S$ = - 15V, $+V_{TH}$ = 5V, $-V_{TH}$ = -5V, R_T = 16.7kΩ, C_T = 1500pF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator								
Initial Accuracy	T_J = 25°C (Note 6)	9.4	10	10.6	9	10	11	kHz
Voltage Stability	V_S = ±5V to ±20V, $V_{PIN\,1}$ = 3V, $V_{PIN\,3}$ = -3V		5	7		5	7	%
Temperature Stability	Over Operating Range (Note 3)		0.5	2		0.5	2	%
$+V_{TH}$ Input Bias Current	$V_{PIN\,2}$ = 6V	-10	0.1	10	-10	0.1	10	µA
$-V_{TH}$ Input Bias Current	$V_{PIN\,2}$ = 0V	-10	-0.5		-10	-0.5		µA
$+V_{TH}$, $-V_{TH}$ Input Range		$+V_S$-2		$-V_S$+2	$+V_S$-2		$-V_S$+2	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 0V		1.5	5		1.5	10	mV
Input Bias Current	V_{CM} = 0V		0.5	5		0.5	5	µA
Input Offset Current	V_{CM} = 0V		0.1	1		0.1	1	µA
Common Mode Range	V_S = ±2.5 to 20V	$-V_S$+2		$+V_S$	$-V_S$+2		$+V_S$	V
Open Loop Voltage Gain	R_L = 10k	75	100		80	100		dB
Slew Rate			15			15		V/µs
Unity Gain Bandwidth			2			2		MHz
CMRR	Over Common Mode Range	75	100		75	100		dB
PSRR	V_S = ±2.5 to ±20V	75	110		75	110		dB

E. UNITRODE UC3637 PWM DRIVER IC

UNITRODE

UC1637
UC2637
UC3637

Switched Mode Controller for DC Motor Drive

FEATURES

- Single or Dual Supply Operation
- ±2.5V to ±20V Input Supply Range
- ±5% Initial Oscillator Accuracy; ± 10% Over Temperature
- Pulse-by-Pulse Current Limiting
- Under-Voltage Lockout
- Shutdown Input with Temperature Compensated 2.5V Threshold
- Uncommitted PWM Comparators for Design Flexibility
- Dual 100mA, Source/Sink Output Drivers

DESCRIPTION

The UC1637 is a pulse width modulator circuit intended to be used for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. When used to replace conventional drivers, this circuit can increase efficiency and reduce component costs for many applications. All necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

This monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with ±100mA output stages as standard features. Protection circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5V temperature compensated threshold.

The UC1637 is characterized for operation over the full military temperature range of -55°C to +125°C, while the UC2637 and UC3637 are characterized for -25°C to +85°C and 0°C to +70°C, respectively.

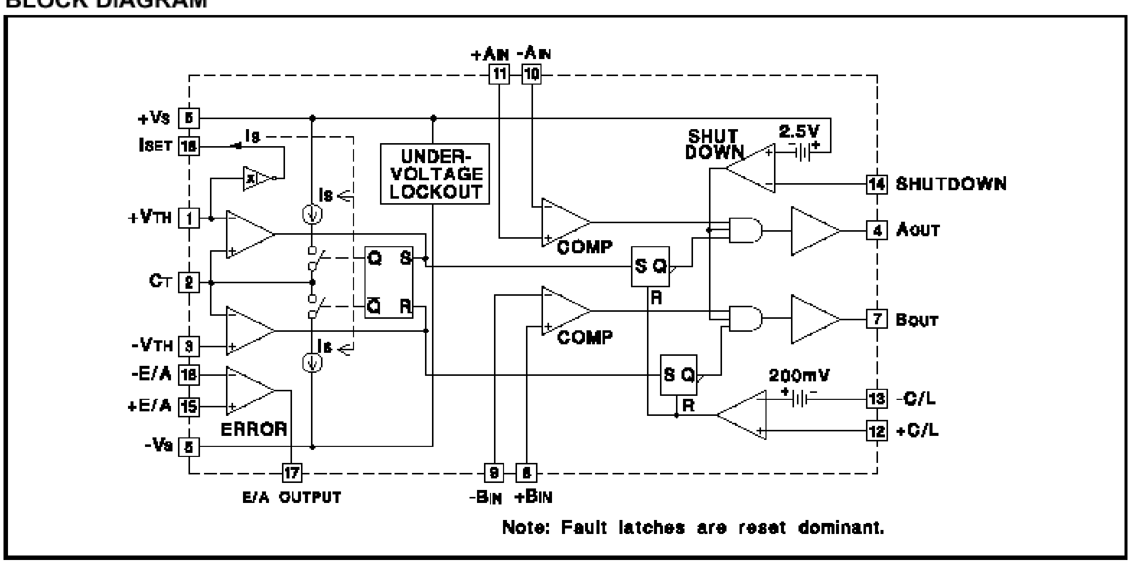
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (±Vs)	±20V
Output Current, Source/Sink (Pins 4, 7)	500mA
Analog Inputs (Pins 1, 2, 3, 8, 9, 10, 11 12, 13, 14, 15, 16)	±Vs
Error Amplifier Output Current (Pin 17)	±20mA
Oscillator Charging Current (Pin 18)	-2mA
Power Dissipation at T_A = 25°C (Note 2)	1000mW
Power Dissipation at T_C = 25°C (Note 2)	2000mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	+300°C

Note 1: Currents are positive into, negative out of the specified terminal.

Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

BLOCK DIAGRAM



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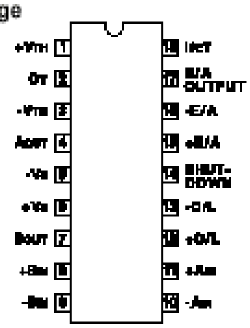
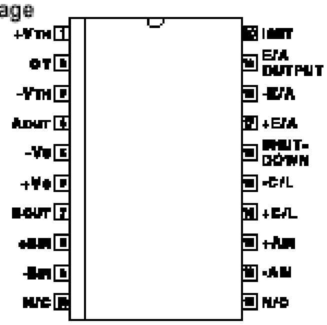
CONNECTION DIAGRAM

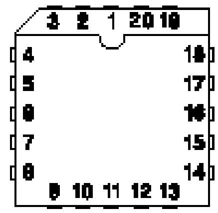
DIL-18 (TOP VIEW)
J or N Package



SOIC-20 (TOP VIEW)
DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
$+V_{TH}$	1
C_T	2
$-V_{TH}$	3
A_{OUT}	4
$-V_S$	5
N/C	6
$+V_S$	7
B_{OUT}	8
$+B_{IN}$	9
$-B_{IN}$	10
$-A_{IN}$	11
$+A_{IN}$	12
+C/L	13
-C/L	14
SHUTDOWN	15
N/C	16
+E/A	17
-E/A	18
E/A OUTPUT	19
I_{SET}	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637; $+V_S$ = +15V, $-V_S$ = - 15V, $+V_{TH}$ = 5V, $-V_{TH}$ = -5V, R_T = 16.7kΩ, C_T = 1500pF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator								
Initial Accuracy	T_J = 25°C (Note 6)	9.4	10	10.6	9	10	11	kHz
Voltage Stability	V_S = ±5V to ±20V, $V_{PIN\ 1}$ = 3V, $V_{PIN\ 3}$ = -3V		5	7		5	7	%
Temperature Stability	Over Operating Range (Note 3)		0.5	2		0.5	2	%
$+V_{TH}$ Input Bias Current	$V_{PIN\ 2}$ = 6V	-10	0.1	10	-10	0.1	10	µA
$-V_{TH}$ Input Bias Current	$V_{PIN\ 2}$ = 0V	-10	-0.5		-10	-0.5		µA
$+V_{TH}$, $-V_{TH}$ Input Range		$+V_S$-2		$-V_S$+2	$+V_S$-2		$-V_S$+2	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 0V		1.5	5		1.5	10	mV
Input Bias Current	V_{CM} = 0V		0.5	5		0.5	5	µA
Input Offset Current	V_{CM} = 0V		0.1	1		0.1	1	µA
Common Mode Range	V_S = ±2.5 to 20V	$-V_S$+2		$+V_S$	$-V_S$+2		$+V_S$	V
Open Loop Voltage Gain	R_L = 10k	75	100		80	100		dB
Slew Rate			15			15		V/µs
Unity Gain Bandwidth			2			2		MHz
CMRR	Over Common Mode Range	75	100		75	100		dB
PSRR	V_S = ±2.5 to ±20V	75	110		75	110		dB

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637: V_S = +15V, $-V_S$ = - 15V, $+V_{TH}$ = 5V, $-V_{TH}$ = -5V, R_T = 16.7kΩ, C_T = 1500pF, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier (Continued)								
Output Sink Current	$V_{PIN\ 17}$ = 0V		-50	-20		-50	-20	mA
Output Source Current	$V_{PIN\ 17}$ = 0V	5	11		5	11		mA
High Level Output Voltage		13	13.6		13	13.6		V
Low Level Output Voltage			-14.8	-13		-14.8	-13	V
PWM Comparators								
Input Offset Voltage	V_{CM} = 0V		20			20		mV
Input Bias Current	V_{CM} = 0V		2	10		2	10	µA
Input Hysteresis	V_{CM} = 0V		10			10		mV
Common Mode range	V_S = ±5V to ±20V	$-V_S$+1		$+V_S$-2	$-V_S$+1		$+V_S$-2	V
Current Limit								
Input Offset Voltage	V_{CM} = 0V, T_J = 25°C	190	200	210	180	200	220	mV
Input Offset Voltage T.C.			-0.2			-0.2		mV/°C
Input Bias Current		-10	-1.5		-10	-1.5		µA
Common Mode Range	V_S = ±2.5V to ±20V	$-V_S$		$+V_S$-3	$-V_S$		$+V_S$-3	V
Shutdown								
Shutdown Threshold	(Note 4)	-2.3	-2.5	-2.7	-2.3	-2.5	-2.7	V
Hysteresis			40			40		mV
Input Bias Current	$V_{PIN\ 14}$ = $+V_S$ to $-V_S$	-10	-0.5		-10	-0.5		µA
Under-Voltage Lockout								
Start Threshold	(Note 5)		4.15	5.0		4.15	5.0	V
Hysteresis			0.25			0.25		mV
Total Standby Current								
Supply Current			8.5	15		8.5	15	mA
Output Section								
Output Low Level	I_{SINK} = 20mA		-14.9	-13		-14.9	-13	V
	I_{SINK} = 100mA		-14.5	-13		-14.5	-13	
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	12	13.5		12	13.5		
Rise Time	(Note 3) C_L = Inf, T_J = 25°C		100	600		100	600	ns
Fall Time	(Note 3) C_L = Inf, T_J = 25°C		100	300		100	300	ns

Note 3: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 4: Parameter measured with respect to +Vs (Pin 6).
Note 5: Parameter measured at +Vs (Pin 6) with respect to -Vs (Pin 5).
Note 6: R_T and C_T referenced to Ground.

FUNCTIONAL DESCRIPTION

Following is a description of each of the functional blocks shown in the Block Diagram.

Oscillator

The oscillator consists of two comparators, a charging and discharging current source, a current source set terminal, I_{SET} and a flip-flop. The upper and lower threshold of the oscillator waveform is set externally by applying a voltage at pins $+V_{TH}$ and $-V_{TH}$ respectively. The $+V_{TH}$ terminal voltage is buffered internally and also applied to the I_{SET} terminal to develop the capacitor charging current through R_T. If R_T is referenced to $-V_S$ as shown in Figure 1, both the threshold voltage and charging current will vary proportionally to the supply differential, and the oscillator frequency will remain constant. The triangle waveform oscillators frequency and voltage amplitude is determined by the external components using the formulas given in Figure 1.

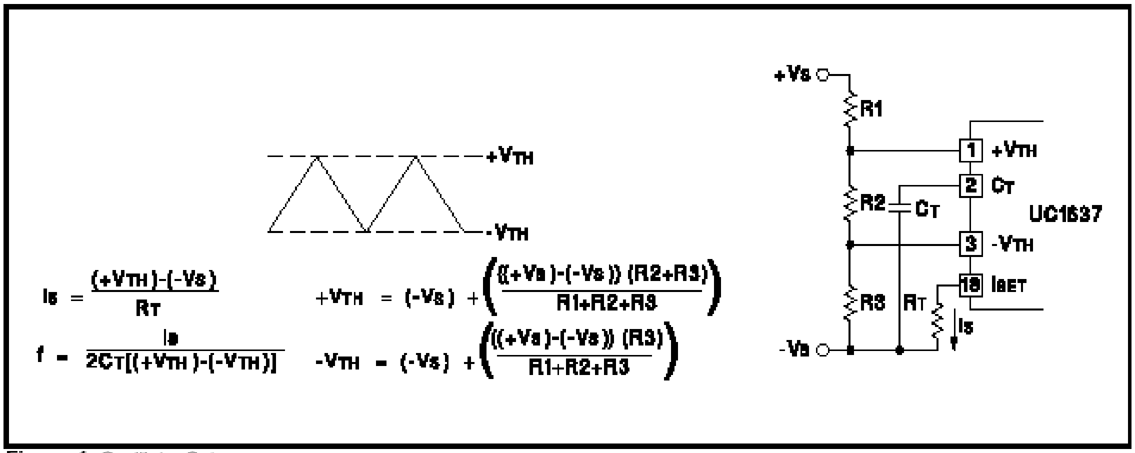


Figure 1. Oscillator Setup

PWM Comparators

Two comparators are provided to perform pulse width modulation for each of the output drivers. Inputs are uncommitted to allow maximum flexibility. The pulse width of the outputs A and B is a function of the sign and amplitude of the error signal. A negative signal at Pin 10 and 8 will lengthen the high state of output A and shorten the high state of output B. Likewise, a positive error signal reverses the procedure. Typically, the oscillator waveform is compared against the summation of the error signal and the level set on Pin 9 and 11.

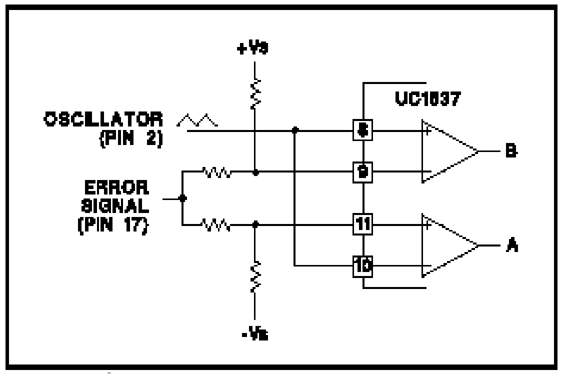


Figure 2. Comparator Biasing

MODULATION SCHEMES

Case A Zero Deadtime (Equal voltage on Pin 9 and Pin 11)
In this configuration, maximum holding torque or stiffness and position accuracy is achieved. However, the power input into the motor is increased. Figure 3A shows this configuration.

Case B Small Deadtime (Voltage on Pin 9 > Pin 11)
A small differential voltage between Pin 9 and 11 provides the necessary time delay to reduce the chances of momentary short circuit in the output stage during transitions, especially where power-amplifiers are used. Refer to Figure 3B.

Case C Increased Deadtime and Deadband Mode
(Voltage on Pin 9 > Pin 11)
With the reduction of stiffness and position accuracy, the power input into the motor around the null point of the servo loop can be reduced or eliminated by widening the window of the comparator circuit to a degree of acceptance. Where position accuracy and mechanical stiffness is unimportant, deadband operation can be used. This is shown in Figure 3C.

Output Drivers

Each output driver is capable of both sourcing and sinking 100mA steady state and up to 500mA on a pulsed basis for rapid switching of either POWERFET or bipolar transistors. Output levels are typically $-V_S + 0.2V$ @50mA low level and $+V_S - 2.0V$ @50mA high level.

Error Amplifier

The error amplifier consists of a high slew rate (15V/µs) op-amp with a typical 1MHz bandwidth and low output impedance. Depending on the $\pm V_S$ supply voltage, the common mode input range and the voltage output swing is within 2V of the V_S supply.

Under-Voltage Lockout

An under-voltage lockout circuit holds the outputs in the low state until a minimum of 4V is reached. At this point, all internal circuitry is functional and the output drivers are enabled. If external circuitry requires a higher starting voltage, an over-riding voltage can be programmed through the shutdown terminal as shown in Figure 4.

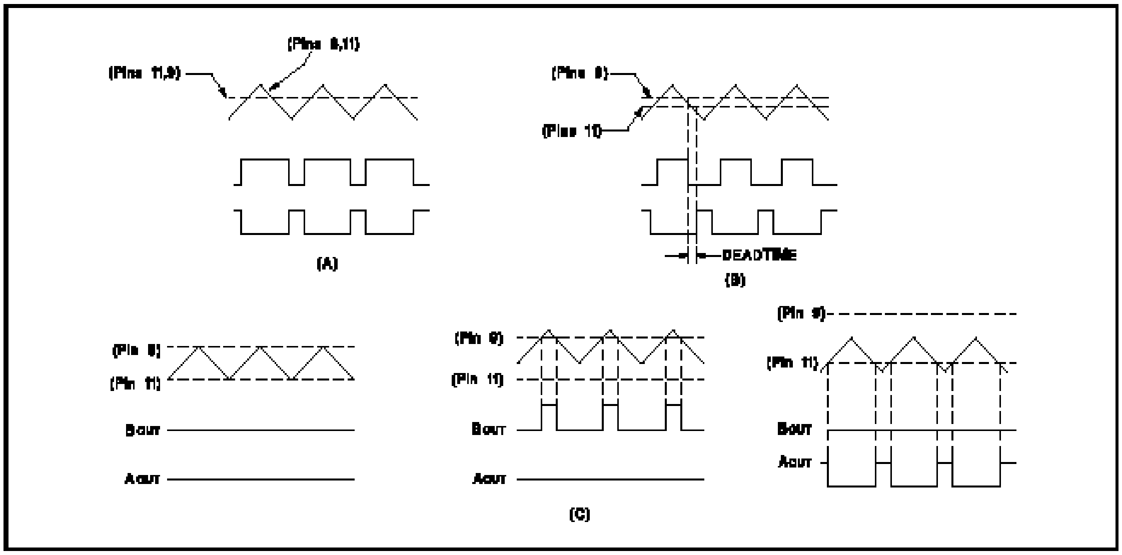


Figure 3. Modulation Schemes Showing (A) Zero Deadtime (B) Deadtime and (C) Deadband Configurations

Shutdown Comparator

The shutdown terminal may be used for implementing various shutdown and protection schemes. By pulling the terminal more than 2.5V below V_{IN}, the output drivers will be enabled. This can be realized using an open collector gate or NPN transistor biased to either ground or the negative supply. Since the threshold is temperature stabilized, the comparator can be used as an accurate low voltage lockout (Figure 4) and/or delayed start as in Figure 5. In the shutdown mode the outputs are held in the low state.

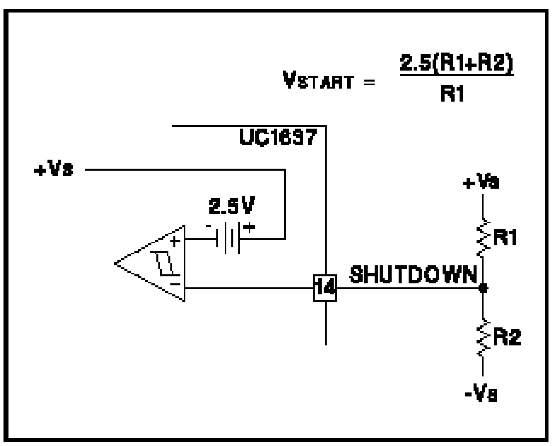


Figure 4. External Under-Voltage Lockout

Current Limit

A latched current limit amplifier with an internal 200mV offset is provided to allow pulse-by-pulse current limiting. Differential inputs will accept common mode signals from

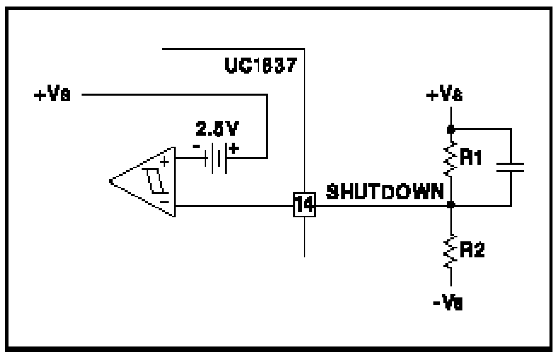


Figure 5. Delayed Start-Up

$-V_S$ to within 3V of the $+V_S$ supply while providing excellent noise rejection. Figure 6 shows a typical current sense circuit.

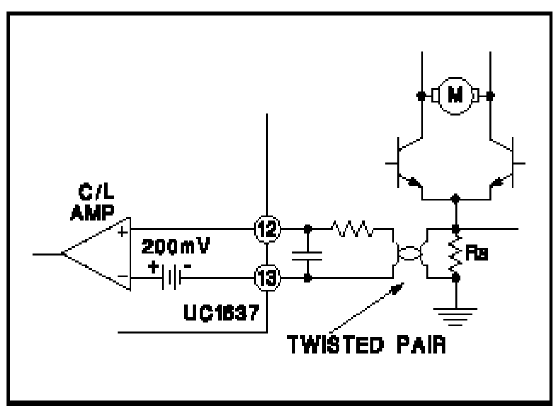


Figure 6. Current Limit Sensing

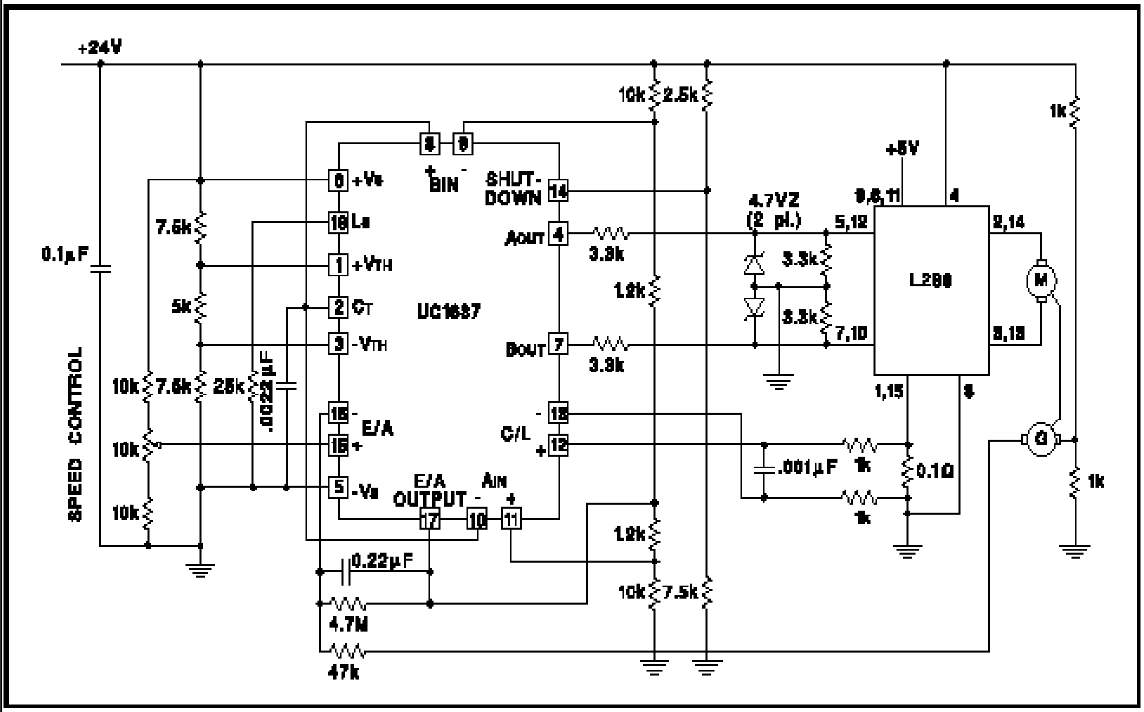


Figure 7. Bi-Directional Motor Drive with Speed Control Power-Amplifier

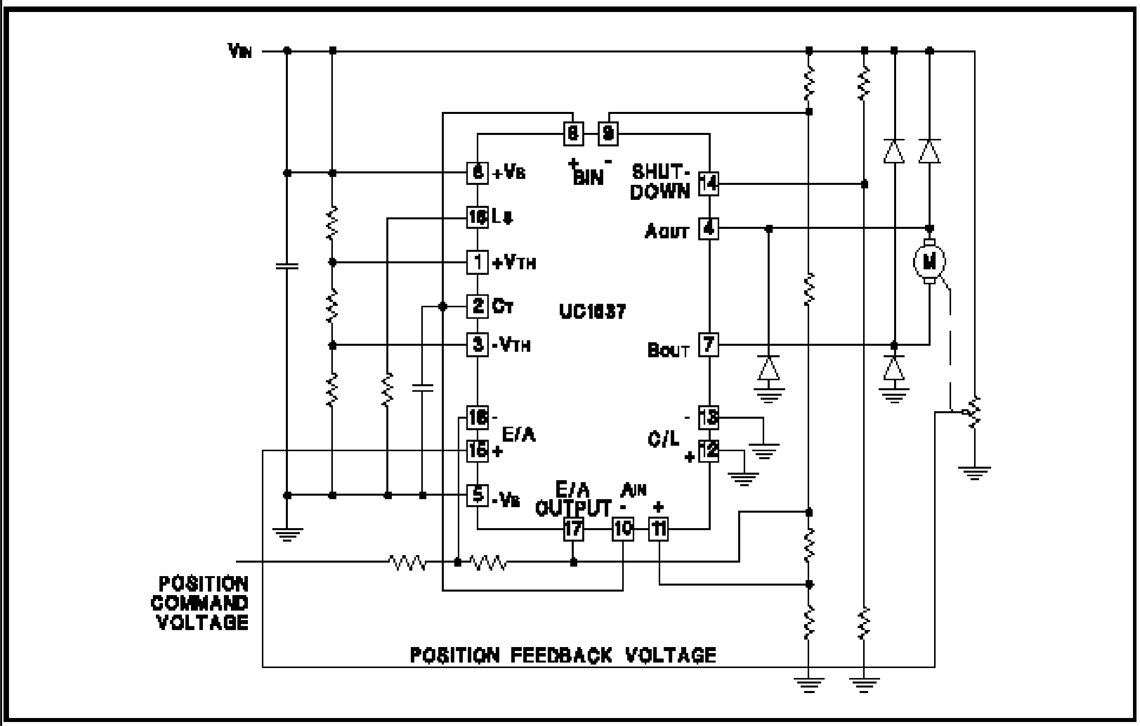
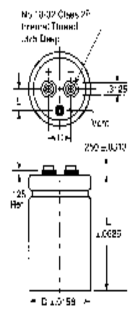


Figure 8. Single Supply Position Servo Motor Drive

F. MALLORY ELECTROLYTIC CAPACITOR

NACC Specification Sheet
For Reference Only

Part Number:	CGH102T450V3L	**Product Type:**	CGH
Capacitance (µF):	1,000	**Operating Temperature (°C):**	-40 to +85
Working Volts (WVDC):	450	**Surge Volts (SVDC):**	525
Tolerance (±%):	-10% +75%		
Sleeve Material:	Blue PVC	**Thickness:**	.008"



Max ESR @ 120Hz - 25°C (MOhms):	83.4
Max ESR @ 20KHz - 25°C (MOhms):	53.4
Max Iac @ 120Hz - 85°C (RMS Amps):	4.8
Max Ripple @ 20KHz - 85°C (RMS Amps):	6.0

Max DC Leakage Current:

I = .006 $\sqrt{CV}$ after 5 Minutes
Not to exceed 6 mA

- C = Capacitance in µF
- V = Rated Voltage
- I = Leakage Current in mA

Dimensions		
	Millimeters	Inches
D		2.000
L		3.625
C		
E		

Performance Specifications

After application of rated DC voltage for 1000 hours at + 85°C.

- CAP ≤10 % from initial measurement
- DF ≤175 % from initial measurement
- DCL initial specified limits

Ripple Multipliers
The maximum ripple current at 85°C and 120 Hz is shown in the Stanard Rating Table.
Maximum ripple current may be adjusted by the multipliers in the following tables.

Rated WVDC	Ripple Multipliers				
	120Hz	400Hz	1KHz	2.5KHz	10KHz
250 to 500	1.000	1.080	1.113	1.175	1.230

Ambient Temp.	Ripple Multiplier
+85°C	1.00
+75°C	1.40
+65°C	1.70

Ambient Temp.	Ripple Multiplier
+55°C	2.00
+45°C	2.25
+35°C	2.45

Other Information

Shelf Life Test: Use a circulating air oven as above for rated shelf life ± 6 hours. Allow capacitors to cool to room temperature and stabilize for a minimum of 16 hours. Capacitance, ESR and DCL will meet initial requirements.

Shelf Life: Capacitors stored more than 5 years should be checked for DCL to see if they meet requirements. Apply rated VDC for 30 minutes through a 1000 Ohm resister to bring DCL within limits.

G. CLN-50 CURRENT SENSORS

Model CLN-50/100

Description

Models CLN-50 and CLN-100 are closed loop Hall effect current sensors that accurately measure dc and ac current and provide electrical isolation between the current carrying conductor and the output of the sensor.

Electrical Specifications

Electrical Specifications	CLN-50		CLN-100	
Nominal current (I_N)	50 A rms		100 A rms	
Measuring range	0 to ± 90 A		0 to ± 150 A	
Sense resistor	**R. min.**	**R. max.**	**R. min.**	**R. max.**
with ± 12 V at ± 70 A peak	50 ohms	90 ohms	n/a	n/a
at ± 100 A peak	n/a	n/a	30 ohms	55 ohms
at ± 150 A peak	n/a	n/a	10 ohms	25 ohms
with ± 15 V at ± 90 A peak	70 ohms	100 ohms	n/a	n/a
at ± 100 A peak	n/a	n/a	30 ohms	85 ohms
at ± 150 A peak	n/a	n/a	30 ohms	40 ohms
Nominal analog output current	50 mA		100 mA	
Turns ratio	1:1000		1:1000	
Overall accuracy at 25 °C and ± 12 V	± 0.9% of I_N		± 0.9% of I_N	
Overall accuracy at 25 °C and ± 15 V	± 0.5% of I_N		± 0.5% of I_N	
Supply voltage (Vdc)	± 12 to ± 15 (± 5%)		± 12 to ± 15 (± 5%)	
Dielectric strength (between the current carrying conductor and the output of the sensor)	3 kV rms/50 Hz/1 min.		3 kV rms/50 Hz/1 min.	

Accuracy-Dynamic Performance

	CLN-50	CLN-100
Zero current offset at 25 °C	± 0.2 mA max.	± 0.2 mA max.
Offset current temperature drift		
between 0 °C and +70 °C	± 0.3 mA typ., ± 0.6 mA max.	± 0.3 mA typ., ± 0.6 mA max.
between -25 °C and +85 °C	± 0.3 mA typ., ± 0.8 mA max.	± 0.3 mA typ., ± 0.8 mA max.
Linearity	better than ±0.1%	better than ±0.1%
Response time	less than 500 ns	less than 500 ns
di/dt accurately followed	better than 100 A/µs	better than 100 A/µs
Bandwidth	0 to 150 kHz (-1 dB)	0 to 150 kHz (-1 dB)

General Information

	CLN-50	CLN-100
Operating temperature	-40 °C to +85 °C	-40 °C to +85 °C
Storage temperature	-40 °C to +90 °C	-40 °C to +90 °C
Current drain (plus output current)	10 mA (at ± 15 V)	14 mA (at ± 15 V)
Coil resistance		
at + 70 °C	30 ohms	30 ohms
at + 85 °C	35 ohms	35 ohms
Package	Flame retarded plastic case	
Weight	18 grams	21 grams
Mounting	Designed to mount on PCB via thru hole connection pins	
Aperture	0.530" x 0.390" (13.5 mm x 10 mm)	
Output reference	To obtain a positive output on the terminal marked "O/P", aperture current must flow in the direction of the arrow (conventional flow)	

Notes

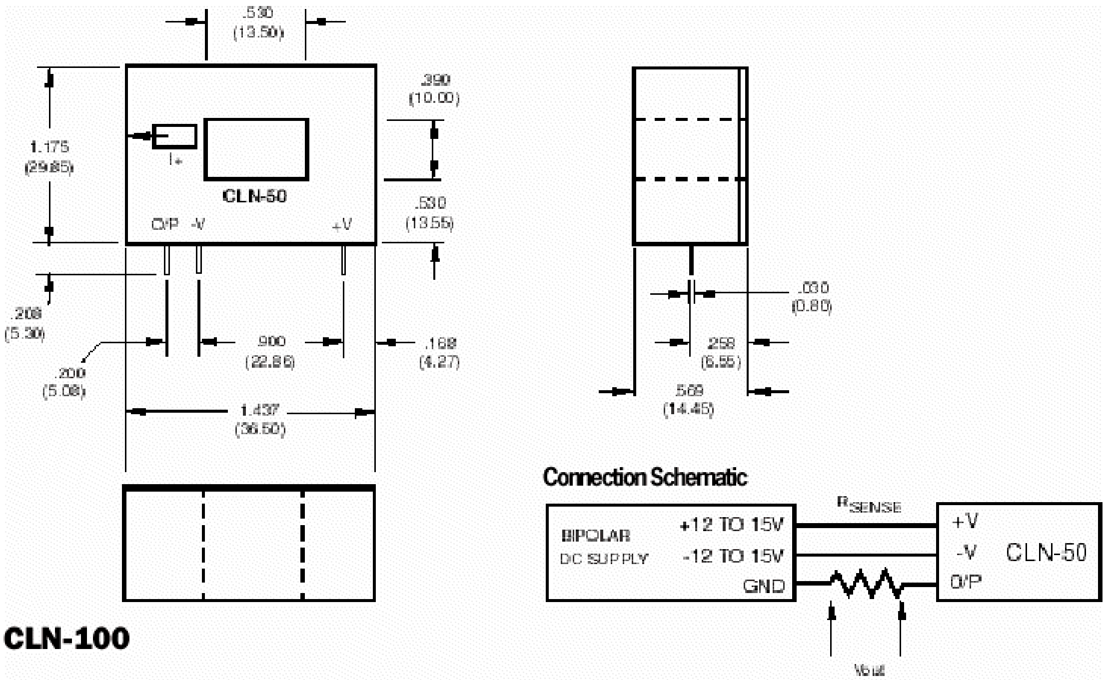
1. The temperature of the current carrying conductor should not exceed 90°C
2. Due to continuous process improvement, all specifications listed in this catalog subject to change without notice.

Model CLN-50/100

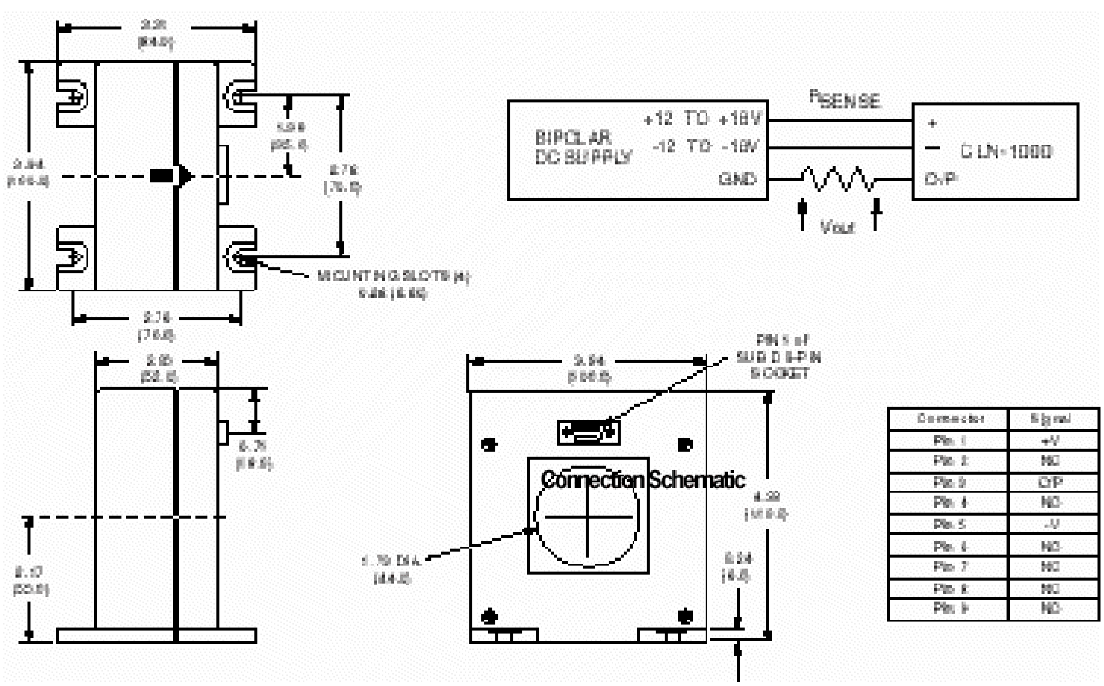
Mechanical Dimensions

All dimensions are in inches (millimeters)

CLN-50



CLN-100



Connector	Signal
Pin 1	+V
Pin 2	NC
Pin 3	O/P
Pin 4	NC
Pin 5	-V
Pin 6	NC
Pin 7	NC
Pin 8	NC
Pin 9	NC

H. ANALOG DEVICES LOW DISTORTION ISOLATION AMP

ANALOG DEVICES

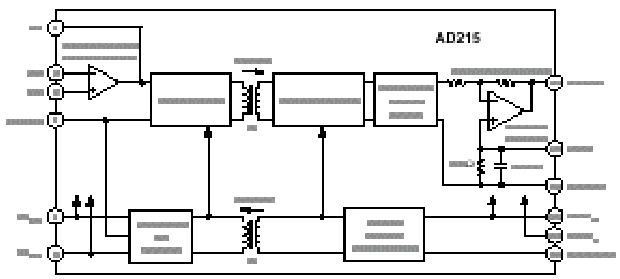
120 kHz Bandwidth, Low Distortion, Isolation Amplifier

AD215

FEATURES
Isolation Voltage Rating: 1,500 V rms
Wide Bandwidth: 120 kHz, Full Power (–3 dB)
Rapid Slew Rate: 6 V/μs
Fast Settling Time: 9 μs
Low Harmonic Distortion: –80 dB @ 1 kHz
Low Nonlinearity: ±0.005%
Wide Output Range: ±10 V, min (Buffered)
Built-In Isolated Power Supply: ±15 V dc @ ±10 mA
Performance Rated over –40°C to +85°C

APPLICATIONS INCLUDE
High Speed Data Acquisition Systems
Power Line and Transient Monitors
Multichannel Muxed Input Isolation
Waveform Recording Instrumentation
Power Supply Controls
Vibration Analysis

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD215 is a high speed input isolation amplifier designed to isolate and amplify wide bandwidth analog signals. The innovative circuit and transformer design of the AD215 ensures wideband dynamic characteristics while preserving key dc performance specifications.

The AD215 provides complete galvanic isolation between the input and output of the device including the user-available front-end isolated power supplies. The functionally complete design, powered by a ±15 V dc supply, eliminates the need for a user supplied isolated dc/dc converter. This permits the designer to minimize circuit overhead and reduce overall system design complexity and component costs.

The design of the AD215 emphasizes maximum flexibility and ease of use in a broad range of applications where fast analog signals must be measured under high common-mode voltage (CMV) conditions. The AD215 has a ±10 V input/output range, a specified gain range of 1 V/V to 10 V/V, a buffered output with offset trim and a user-available isolated front-end power supply which produces ±15 V dc at ±10 mA.

PRODUCT HIGHLIGHTS

High Speed Dynamic Characteristics: The AD215 features a typical full-power bandwidth of 120 kHz (100 kHz min), rise time of 3 μs and settling time of 9 μs. The high speed performance of the AD215 allows for unsurpassed galvanic isolation of virtually any wideband dynamic signal.

Flexible Input and Buffered Output Stages: An uncommitted op amp is provided on the input stage of the AD215 to allow for input buffering or amplification and signal conditioning. The AD215 also features a buffered output stage to drive low impedance loads and an output voltage trim for zeroing the output offset where needed.

High Accuracy: The AD215 has a typical nonlinearity of ±0.005% (B grade) of full-scale range and the total harmonic distortion is typically –80 dB at 1 kHz. The AD215 provides designers with complete isolation of the desired signal without loss of signal integrity or quality.

Excellent Common-Mode Performance: The AD215BY (AD215AY) provides 1,500 V rms (750 V rms) common-mode voltage protection from its input to output. Both grades feature a low common-mode capacitance of 4.5 pF inclusive of the dc/dc power isolation. This results in a typical common-mode rejection specification of 105 dB and a low leakage current of 2.0 μA rms max (240 V rms, 60 Hz).

Isolated Power: An unregulated isolated power supply of ±15 V dc @ ±10 mA is available at the isolated input port of the AD215. This permits the use of ancillary isolated front-end amplifiers or signal conditioning components without the need for a separate dc/dc supply. Even the excitation of transducers can be accomplished in most applications.

Rated Performance over the –40°C to +85°C Temperature Range: With an extended industrial temperature range rating, the AD215 is an ideal isolation solution for use in many industrial environments.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD215–SPECIFICATIONS (Typical @ +25°C, V_S = ±15 V dc, 2 kΩ output load, unless otherwise noted.)

Parameter	Conditions	AD215AY/BY Min	Typ	Max	Units
GAIN					
Range[1]		1		10	V/V
Error	G = 1 V/V, No Load on V_{ISO}		±0.5	±2	%
vs. Temperature	0°C to +85°C		+15		ppm/°C
	–40°C to 0°C		+50		ppm/°C
vs. Supply Voltage	±(14.5 V dc to 16.5 V dc)		+100		ppm/V
vs. Isolated Supply Load[2]			+20		ppm/mA
Nonlinearity[3]					
AD215BY Grade	±10 V Output Swing, G = 1 V/V		±0.005	±0.015	%
	±10 V Output Swing, G = 10 V/V		±0.01		%
AD215AY Grade	±10 V Output Swing, G = 1 V/V		±0.01	± 0.025	%
	±10 V Output Swing, G = 10 V/V		±0.025		%
INPUT VOLTAGE RATINGS					
Input Voltage Rating	G = 1 V/V	±10			V
Maximum Safe Differential Range	IN+ or IN–, to IN COM		±15		V
CMRR of Input Op Amp			100		dB
Isolation Voltage Rating[4]	Input to Output, AC, 60 Hz				
AD215BY Grade	100% Tested[4]	1500			V rms
AD215AY Grade	100% Tested[4]	750			V rms
IMRR (Isolation Mode Rejection Ratio)	R_S ≤ 100 Ω (IN+ & IN–), G = 1 V/V, 60 Hz		120		dB
	R_S ≤ 100 Ω (IN+ & IN–), G = 1 V/V, 1 kHz		100		dB
	R_S ≤ 100 Ω (IN+ & IN–), G = 1 V/V, 10 kHz		80		dB
	R_S ≤ 1 kΩ (IN+ & IN–), G = 1 V/V, 60 Hz		105		dB
	R_S ≤ 1 kΩ (IN+ & IN–), G = 1 V/V, 1 kHz		85		dB
	R_S ≤ 1 kΩ (IN+ & IN–), G = 1 V/V, 10 kHz		65		dB
Leakage Current, Input to Output	240 V rms, 60 Hz			2	µA rms
INPUT IMPEDANCE					
Differential	G = 1 V/V		16		MΩ
Common Mode			2‖4.5		GΩ‖pF
INPUT OFFSET VOLTAGE					
Initial	@ +25°C		±0.4	±2.0	mV
vs. Temperature	0°C to +85°C		±2		µV/°C
	–40°C to 0°C		±20		µV/°C
OUTPUT OFFSET VOLTAGE					
Initial	@ +25°C, Trimmable to Zero	0	–35	–80	mV
vs. Temperature	0°C to +85°C		±30		µV/°C
	–40°C to 0°C		±80		µV/°C
vs. Supply Voltage			±350		µV/V
vs. Isolated Supply Load[2]			–35		µV/mA
INPUT BIAS CURRENT					
Initial	@ +25°C		300		nA
vs. Temperature	–40°C to +85°C		±400		nA
INPUT DIFFERENCE CURRENT					
Initial	@ +25°C		±3		nA
vs. Temperature	–40°C to +85°C		±40		nA
INPUT VOLTAGE NOISE					
Input Voltage Noise	Frequency > 10 Hz		20		$nV/\sqrt{Hz}$
DYNAMIC RESPONSE (2 kΩ Load)					
Full Signal Bandwidth (–3 dB)	G = 1 V/V, 20 V pk-pk Signal	100	120		kHz
Transport Delay[6]			2.2		µs
Slew Rate	±10 V Output Swing		6		V/µs
Rise Time	10% to 90%, ±10 V Output Swing		3		µs

Parameter	Conditions	AD215AY/BY Min	Typ	Max	Units
DYNAMIC RESPONSE (2 kΩ Load) Cont.					
Settling Time	to ±0.10%, ±10 V Output Swing		9		μs
Overshoot			1		%
Harmonic Distortion Components	@ 1 kHz		–80		dB
	@ 10 kHz		–65		dB
Overload Recovery Time	G = 1 V/V, ±15 V Drive		5		μs
Output Overload Recovery Time	G > 5		10		μs
RATED OUTPUT					
Voltage	Out HI to Out LO	±10			V
Current	2 kΩ Load	±5			mA
Max Capacitive Load			500		pF
Output Resistance			1		Ω
Output Ripple and Noise[7]	1 MHz Bandwidth		10		mV pk-pk
	50 kHz Bandwidth		2.5		mV pk-pk
ISOLATED POWER OUTPUT[8]					
Voltage	No Load	±14.25	±15	±17.25	V
vs. Temperature	0°C to +85°C		+20		mV/°C
	–40°C to 0°C		+25		mV/°C
Current at Rated Supply Voltage[2, 9]			±10		mA
Regulation	No Load to Full Load		–90		mV/V
Line Regulation			290		mV/V
Ripple	1 MHz Bandwidth, No Load[2]		50		mV rms
POWER SUPPLY					
Supply Voltage	Rated Performance	±14.5	±15	±16.5	V dc
	Operating[10]	±14.25		±17	V dc
Current	Operating (+15 V dc/–15 V dc Supplies)		+40/–18		mA
TEMPERATURE RANGE					
Rated Performance		–40		+85	°C
Storage		–40		+85	°C

NOTES

[1]The gain range of the AD215 is specified from 1 to 10 V/V. The AD215 can also be used with gains of up to 100 V/V. With a gain of 100 V/V a 20% reduction in the –3 dB bandwidth specification occurs and the nonlinearity degrades to ±0.02% typical.

[2]When the isolated supply load exceeds ±1 mA, external filter capacitors are required in order to ensure that the gain, offset, and nonlinearity specifications are preserved and to maintain the isolated supply full load ripple below the specified 50 mV rms. A value of 6.8 μF is recommended.

[3]Nonlinearity is specified as a percent (of full-scale range) deviation from a best straight line.

[4]The isolation barrier (and rating) of every AD215 is 100% tested in production using a 5 second partial discharge test with a failure detection threshold of 150 pC. All "B" grade devices are tested with a minimum voltage of 1,800 V rms. All "A" grade devices are tested with a minimum voltage of 850 V rms.

[5]The AD215 should be allowed to warm up for approximately 10 minutes before any gain and/or offset adjustments are made.

[6]Equivalent to a 0.8 degrees phase shift.

[7]With the ±15 V dc power supply pins bypassed by 2.2 μF capacitors at the AD215 pins.

[8]Caution: The AD215 design does not provide short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

[9]With an input power supply voltage greater than or equal ±15 V dc, the AD215 may supply up to ±15 mA from the isolated power supplies.

[10]Voltages less than 14.25 V dc may cause the AD215 to cease operating properly. Voltages greater than ±17.5 V dc may damage the internal components of the AD215 and consequently should not be used.

Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD215 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

I. NATIONAL SEMICONDUCTOR QUAD 2-INPUT OR GATE

National Semiconductor

February 1988

CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate

General Description

These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

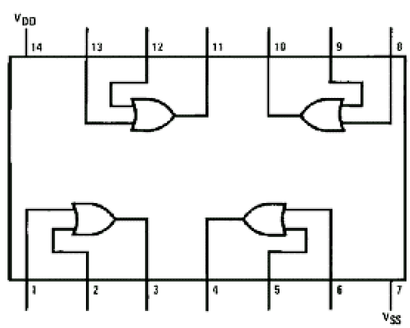
All inputs protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagrams

CD4071B Dual-In-Line Package



Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$-0.5V$ to $V_{DD} + 0.5V$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
V_{DD} Range	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Storage Temperature (T_S)	$-65°C$ to $+150°C$
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

Operating Range (V_{DD})	$3\ V_{DC}$ to $15\ V_{DC}$
Operating Temperature Range (T_A)	
CD4071BM, CD4081BM	$-55°C$ to $+125°C$
CD4071BC, CD4081BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4071BM/CD4081BM (Note 2)

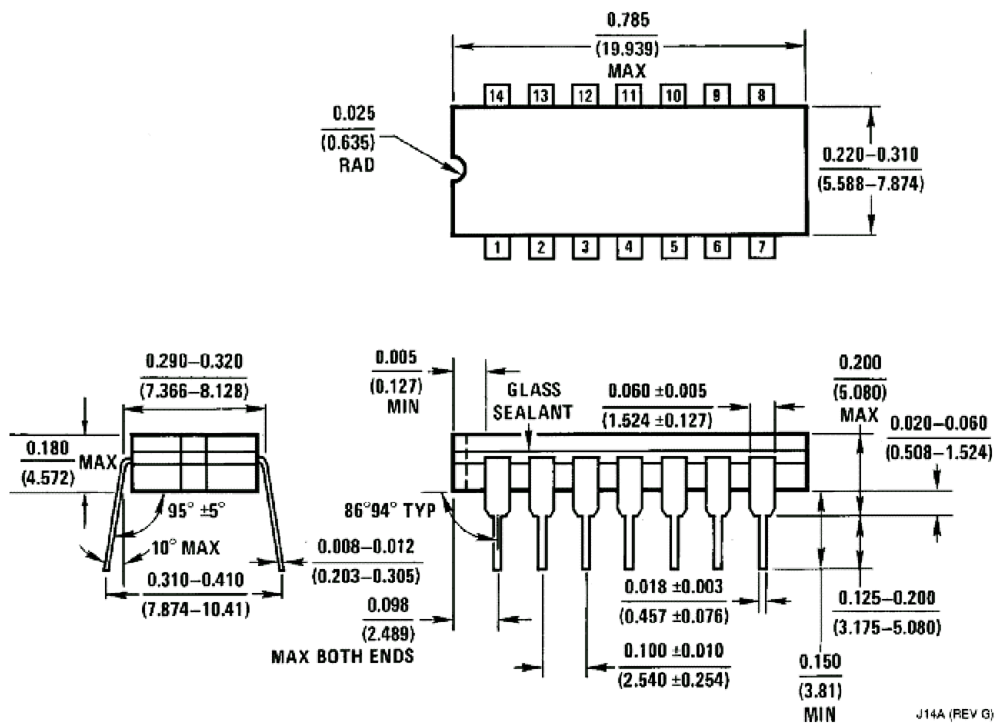
Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10V$		0.50		0.005	0.50		15	μA
		$V_{DD} = 15V$		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$, $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$, $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$, $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V, V_O = 13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4071BMJ, CD4071BCJ
CD4081BMJ or CD4081BCJ
NS Package Number J14A

APPENDIX B. MATLAB CODE

A. BUCK CONVERTER

The following MATLAB m-files were utilized in the design of the buck chopper.

1. MATLAB M-file (BUCK_closeloop_bessel.m)

This m-file is used to determine gains, required control circuit resistance, open and closed-loop transfer functions, and various plots.

```
%*******************************************************************
% BUCK_closeloop_bessel.m
%
% Specifications:
% 100A IGBT's
% Stable and continuous operation between 10% and 100% load
%
% This program calculates the required gains of the
% control circuitry and evaluates the open and closed-
% loop transfer function of the buck chopper.  User
% inputs desired load resistance and program calculates
% required gains, resistor components, step responses, and
% bode plots.
%
% Written by; Brad L. Stallings 12-18-2000
% Last mod:  April 2001
%*******************************************************************

clear
format long
format compact

%*******************************************************************
% Constants defined
%*******************************************************************

R=input('Input Load resistance ')
T=1/20000;                          % switching time
E=500                               % input voltage
```

```
d=400/E                          % duty cycle
L=1e-3                           % output inductor size
C=500e-6                         % output capacitor size
w=2*pi*500;                      % control bandwidth


%*********************************************************************
% Desired pole specification (bessel)
%*********************************************************************

poles=w*[-0.7455+j*0.7112,-0.7455-j*0.7112,-0.9420]
S=poly(poles)                    % polynomial equation
S1=S(1);                         % coefficient one
S2=S(2);                         % coefficient two
S3=S(3);                         % coefficient three
S4=S(4);                         % coefficient four

%*********************************************************************
% Gain calculations
%*********************************************************************

hi=L/E*(S(2)-1/(R*C))            % current gain
hv=((L*C)/E)*(S(3)-1/(L*C))      % voltage gain
hn=(S(4)*L*C)/E                  % integral gain

%*********************************************************************
% Solve for unknown resistor values for control circuit.
%*********************************************************************

R101=10000                             % ohm see Figure (5-7)
R102B=10000                            % ohm
R102C=10000                            % ohm
R106=10000                             % ohm
R108=10000                             % ohm
R109=10000                             % ohm
R110=10000                             % ohm
R112G=10000                            % ohm
C107=0.1e-6                            % 0.1 micro farad
R113B=150000                           % ohm
R114=(50*R113B)*hi                     % ohm
R113C=(R114)/(1000*C107*R106*hn)       % ohm
r=1000*hv;
r1=(R113B*R113C)/(R113B+R113C);
R112=((r1+R114)*R112G)/(hv*1000*r1)-R112G    % ohm
```

```
%*****************************************************************
% This section calculates the Transfer functions of Buck
% Converter (both open and closed-loop and displays various plots.
%*****************************************************************

b1=1/(R*C);                          % b1, b2, b3 defined

b2=E/(L*C);
b3=1/(L*C);
n1=[b2*hv,b2*hn];                    % numerator terms closed-loop
d1=[1,b1+E/L*hi,b3+b2*hv,b2*hn];     % denominator terms closed-loop
roots_1=roots(d1)                    % roots of denominator closed-loop
sys=tf(n1,d1);                       % transfer function closed-loop

figure (1)
step(sys,.0055);
M=step(sys,.0055);                   % step response for closed-loop

figure (2)
bode(sys);                           % bode plot closed-loop

OS1=max(M)                           % Overshoot Calculation
Percent_Overshoot1=((OS1-1)/(1))*100

%*****************************************************************
% Function to verify poles obtained with the gains
% computed match desired poles
%*****************************************************************

Am=[0 -1/L E/L;1/C -1/(R*C) 0; -hv/C (hi/L)+(hv/(R*C))-hn -hi*E/L]
closed_loop_poles=eig(Am)            % verifies correct poles

%*****************************************************************
%The following code examines the open-loop response
%*****************************************************************

n2=[b2*hv,b2*hn];                    % numerator terms open-loop
d2=[1,b1+E/L*hi,b3,0];               % denominator terms open-loop
roots_2=roots(d2)                    % roots of denominator open-loop
sysopen=tf(n2,d2)                    % transfer function open-loop

figure (3)
bode(sysopen,{1,1e6});               % bode plot open-loop
```

2. MATLAB M-file (Inductance.m)

```
%*********************************************************************
% Inductance.m
%
% Specifications:
% Stable/continuous operation between 10% and 100% load
%
% This program calculates the required inductance for the buck chopper
%  power section.
%
% Written by; Brad L. Stallings 11-11-2000
% Last mod: December 2000
%*********************************************************************

clear
format long
format compact

%*********************************************************************
% Inputs Requested
%*********************************************************************

R=input('Input Load resistance in ohms ')
T=input('Input Switching Time in seconds  ')
E=input('Input Input Voltage in Volts   ')
Vout=input('Input Desired Output Voltage in Volts  ')
le=input('Input Mean length of Magnetic Path from Spec Sheet in cm   ')
I=input('Input DC current through Inductor in Amps  ')
L_1000=input('Input Inductance in mH for 1000 Turns from Spec sheet  ')
Ae=input('Input Cross Sectional Area of Magnetic Path in cm squared from Spec Sheet  ')

F=1/T                                    % Switching Frequency in hertz
D=Vout/E                                 % Duty cycle, dimensionless
Lcrit=((T*R)/2)*(1-D)                    % Critical inductance in henries
L=10*Lcrit                               % Desired inductance in henries
N=1000*(sqrt(L/L_1000))                  % Required number of turns, dimensionless
H=(0.4*pi*N*I)/le                        % Magnetizing force in Oersteds
Bmax=(E/(sqrt(2))*1e8*(1-D))/(N*Ae*F*2)  % Flux density in Gausses
u=(L*le)/(4*pi*Ae*N^2)*1e9               % Calculated Permeability
                                         %( L is in nanohenries)
```

3. MATLAB M-files (Cap_1.m, Cap_2.m Cap_3.m, Plott_x.m)

The following detailed SIMULINK model and four m-files were utilized to investigate the output voltage and inductor current responses. The following steps are utilized to obtain the desired results and all steps must be conducted in the order listed:

- user defines the test capacitor size in the Cap_1.m file,
- execute Cap_1.m file,
- execute detailed model,
- execute Cap_2.m file,
- execute detailed model,
- execute Cap_3.m file,
- execute detailed model,
- execute Plott_x.m.

To access the files above, go under desktop "Thesis" and then to MATLAB files. This project performed several runs for a multitude of capacitor values. Chapter III offered only two runs in order to give the user a visual on how the value of the output capacitance can greatly influence system performance. A time step of 1E-6 must be selected in order to portray information accurately.

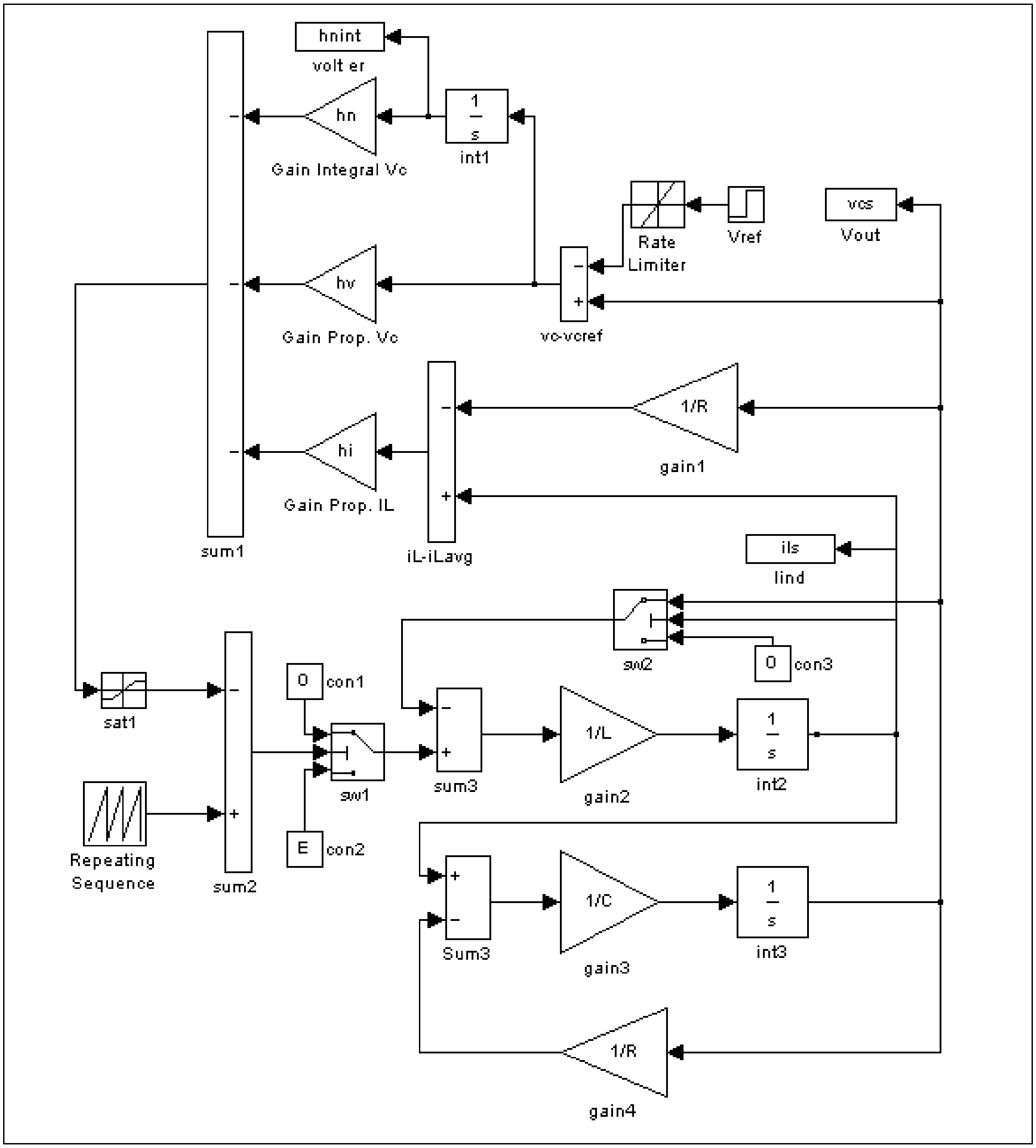


Figure B-1, SIMULINK Detailed Model of Buck Converter.

a. MATLAB M-file (Cap_1.m)

```
%***************************************************************** *****
% Cap_1.m
%
% M-files Cap_1.m, Cap_2.m, and Cap_3.m were written to calculate
% required output capacitance for the SSCM.  The program steps load
% resistance from 10% to 100% and back to 10%.  Cap_1.m is executed
% first, the integrator values that remain at the end of Cap_1.m are
% applied as the initial conditions for Cap_2.m.  The integrator
% values at the end of Cap_2.m are applied as the initial conditions
% to the integrators to Cap_3.m.  After the simulation is is complete,
% Plott_x.m is executed to provide capacitor voltage and inductor
% current plots.
%
% Determining SSCM Circuit Parameters, 8kW SSCM
%
% Written by: Dr. Bob Ashton Naval Postgraduate School and modified
% by Brad Stallings
% Last Mod: March 2001
%******************************************************************

clear all;

T=1/20000;                  % switching time
E=500                       % input voltage
d=400.0/E                   % duty cycle
L=1e-3                      % output inductor size
C=500e-6                    % output capacitor size
w=2*pi*500;                 % control bandwidth
rxlow=1.0;
rxhigh=10.0;
rxstart=1.0;
Rn=200.0;                   % load resistance initial
R=Rn/rxstart                % load resistance
il=(E*d)/R;                 % inductor current


%******************************************************************
% Desired pole specification (bessel)
%******************************************************************

poles=w*[-0.7455+j*0.7112,-0.7455-j*0.7112,-0.9420]; %Bessel pole locations
S=poly(poles)               % polynomial equation
S1=S(1);                    % coefficient one
```

```
S2=S(2);                         % coefficient two
S3=S(3);                         % coefficient three
S4=S(4);                         % coefficient four

%*********************************************************************
% Gain calculations
%*********************************************************************

hi=L/E*(S(2)-1/(R*C))            % current gain
hv=((L*C)/E)*(S(3)-1/(L*C))      % voltage gain
hn=(S(4)*L*C)/E                  % integral gain

%*********************************************************************
% Function to verify poles obtained with gains, match the
% desired poles.
%*********************************************************************

Am=[0              -1/L                        E/L
    1/C            -1/(R*C)                     0
    (-hv/C+hi/R/C) (hi/L+hv/R/C-hi/R/R/C-hn)  (-hi*E/L)];

syspole = eig(Am)/2/pi           % check for correct poles

vcsd=d*E;                        % desired SSCM output voltage
vciv=0.0;                        % initial vcs integrator value
iliv=0.0;                        % initial il integrator value
hnintiv=0.0;                     % initial hn integrator value
tstart=0.0;                      % simulation start time
tstop=0.2;                       % simulation stop time
hnint=0.0;                       % initial integrator value
```

b. MATLAB M-file (Cap_2.m)

```
%**********************************************************************
% Cap_2.m
%
% Parameter variation file for step change analysis.
% New SSCM Parameters
%
% Written by: Dr. Bob Ashton Naval Postgraduate School and modified
% by Brad Stallings
% Last Mod: April 2001
%**********************************************************************

R=Rn/rxhigh;                    % load resistor

%**********************************************************************
% Update initial conditions for integrators (leave these alone).
%**********************************************************************

vciv=vcs(length(time));         % new integrator initial condition
iliv=ils(length(time));         % new integrator initial condition
hnintiv=hnint(length(time));    % new integrator initial condition

%**********************************************************************
% Concatenate paramaters (leave these alone).
%**********************************************************************

timen=[timen' time']';
vcsn=[vcsn' vcs']';
ilsn=[ilsn' ils']';

%**********************************************************************
% New simulation start and stop times (change as desired).
%**********************************************************************

tstart=tstop;                   % new start time
tstop=tstop + 0.03;             % new stop time
```

c. MATLAB M-file (Cap_3.m)

```
%*******************************************************************
% Cap_3.m
%
% Parameter variation file for step change analysis.
%
% Written by: Dr. Bob Ashton Naval Postgraduate School and modified
% by Brad Stallings
% Last Mod: April 2001
%*******************************************************************

R=Rn*rxlow;                    % change load resistance

%*******************************************************************
% Update initial conditions for integrators (leave these alone).
%*******************************************************************

vciv=vcs(length(time));        % new integrator initial conditions
iliv=ils(length(time));        % new integrator initial conditions

%*******************************************************************
% Concatenate parameters (leave these alone).
%*******************************************************************

timen=[timen' time']';
vcsn=[vcsn' vcs']';
ilsn=[ilsn' ils']';

%*******************************************************************
% New simulation start and stop times (change as desired).
%*******************************************************************

tstart=tstop;                  % new start time
tstop=tstop + 0.03;            % new stop time
```

d. MATLAB M-file (Plott_x.m)

```
%****************************************************************
% Plott_x.m
%
% Multi-loop plot file for step responses.
% Run this file after Cap_1.m, Cap_2.m, and Cap_3.m are executed.
%
% Written by: Dr Bob Ashton, modified by Brad Stallings
% Last mod: April 2001
%****************************************************************

timen=[timen' time'];
vcsn=[vcsn' vcs' ];
ilsn=[ilsn' ils'];
leg=length(timen);
from=13000;
subplot(2,1,1);
plot(timen(from:leg),ilsn(from:leg));
title('CAPACITOR VOLTAGE');
axis([0.18 0.26 385 415])
subplot(2,1,2);
plot(timen(from:leg),ilsn(from:leg));
title('INDUCTOR CURRENT');
axis([0.18 0.26 0 35])
```

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APPENDIX C. PARTS LIST

A. BUCK CHOPPER PARTS LIST

The table below provides a list of the major part requirements in the dc-dc converter.

Number Required and Part/Stock number	**Manufacturer**	**Cost**	**Unit of Issue**	**Lead Time**
1-IGBT SKM100GB124D	Semikron	$177.70	EA	4-6 weeks
1-IGBT Driver Board SKI-10/17	Semikron	$51.25	EA	10 days
1-60µ Toroid A-125112-2	Group Arnold	$127.86	EA	7 weeks
1-147µ Toroid A-158304-2	Group Arnold	$175.04	EA	7 weeks
1-18-Pin PWM chip 296-2508-5-ND	Digikey (Verify it is not surface mounted)	$5.28	EA	6 weeks
2-CLN-50 Current Sensor CLN-50	Allied Electronics Inc. (Made by F.W. Bell)	$28.00	EA	10 weeks
2-Capacitor (1000µF/450V) CGH102T450V3L	Newark	$43.08	EA	2 weeks
2-Capacitor (1000µF/350V) 857-0310	Allied Electronics Inc. (Made by Mallory	$19.41	EA	10 weeks
2-Iso-Amplifier (AD-215) 630-8042	Allied Electronics Inc. (Made by Analog Device)	$99.81	EA	10 weeks

Number Required and Part/Stock number	Manufacturer	Cost	Unit of Issue	Lead Time
1-Low Power AC-DC Switches 92F5324	Newark	$50.00	EA	2 weeks
1-Rack Mount Chassis (17"x19"x10.5") 90F6954	Newark	$92.26	EA	2 weeks

B. CONTROL CARD PARTS LIST

Part	Description/Value	Number Required
Resistor	10kΩ *	9
Resistor	55kΩ	1
Resistor	4.7kΩ	1
Resistor	150kΩ	1
Resistor	20kΩ	1
Zener Diode	1N827 or 1N5234/6.2V	2
Capacitor	0.1µF (50V_{dc})	3
Op-Amp	LF347 quad op-amp	1
Jumper	Wire	1

*** All resistors are 1/4 watt**

C. PROTECTION CIRCUITRY PARTS LIST

Part	**Description/Value**	**Number Required**
Resistor	4.7kΩ *	1
Resistor	10kΩ	8
Resistor	27kΩ	1
Resistor	100kΩ	1
Resistor	20kΩ	1
Resistor	30kΩ	3
Resistor	100kΩ	1
Resistor	300Ω	1
Resistor	4.3kΩ	1
Capacitor	0.47μF ($50V_{dc}$)	1
Capacitor	0.1μF ($50V_{dc}$)	5
Capacitor	1.0μF ($50V_{dc}$)	1
Capacitor/electrolytic	10.0μF ($25V_{dc}$)	1
Gate	CD4071/quad OR gate	1
OP-Amp	MC1458	1
Transistor	2N2222A	3

*** All resistors are 1/4 watt**

D. PWM CIRCUIT PARTS LIST

Part	Description/Value	Number Required
Resistor	470Ω *	1
Resistor	4.7kΩ	1
Resistor	1.8kΩ	1
Resistor	9.1kΩ	1
Resistor	27kΩ	1
Resistor	13kΩ	1
Resistor	5.6kΩ	1
Capacitor	0.047μF (50V_{dc})	1
Capacitor	0.47μF (50V_{dc})	2
Capacitor	0.1μF (50V_{dc})	2
Capacitor	2200pF (50V_{dc})	1
Capacitor	1.0μF (50V_{dc})	1
Capacitor	0.22μF (50V_{dc})	1
Zener Diode	1N5240B/10V	2
Diode	1N4148	2
PWM Chip	UC3637 or UC1637	1

*** All resistors are 1/4 watt**

E. POWER SUPPLIES

Part	Description/Value	Number Required
Capacitor (electrolytic)	2200 μF ($50V_{dc}$)	4
Capacitor (ceramic)	0.1 μF, ($25V_{dc}$)	2
Diode (line frequency)	1N4003	4
Voltage regulator	LM 7815 (+15V)	1
Voltage regulator	LM 7915 (-15V)	1
Transformer	36 Vct, 1Amp	1

F. VOLTAGE SENSING CIRCUIT

Part	Description/Value	Number Required
Resistor	2.7kΩ, 2W	2
Zener Diode	1N5240B/10V	2

G. CURRENT SENSOR BOARDS PARTS LIST

Part	Description/Value	Number Required
Resistor	200Ω, 1/4W	2
Current sensor	CL-50	2
Twisted pair wire	yellow/ -15V brown/ground orange/output red/+15V	2 8 2 2

H. BUFFER STAGE

Part	Description/Value	Number Required
Resistor	3.6kΩ, 1/4W	4
Capacitor	2200pF (50V_{dc})	4
Capacitor	0.1μF (50V_{dc})	2
Op-Amp	LF324/quad op-amp	1
Jumper	wire	1

I. FRONT/REAR PANEL PARTS LIST

Part	Description/Value	Number Required
Fuse Holder	125V-3A	1
Fuse Holder	600V-30A	1
Fan Cover	4.7" Globe Accessories	2
Range Plug	250V-30A	1
Plug Male	115V-1A	1
Front Panel Meters	20V/2mA	2
Light Emitting Diode	1mA	4
BNC Connectors	75Ω	5
Potentiometer	1-kΩ	1

J. MISCELLANEOUS

Part	Description/Value	Number Required
Power Supply (For digital meters)	5V Part #(48818) manufacturer (KEPCO)	1
Thermistor Switch	70°C/15V Part #(317-1019-ND) from Digikey	1

APPENDIX D. EASYTRAX LAYOUTS/DATA

A. ANALOG CONTROLLER PRINTED CIRCUIT BOARD DATA

This section is divided into a component parts listing, an EASYTRAX PCB netlist, and a Printed Circuit Board (PCB) and sensor board component overlay.

1. Component List Main PCB Board

Q3
TO-39

Q2
TO-39

Q1
TO-39

R208Z
AXIAL0.3

DA201
DIODE0.4

DA101
DIODE0.4

RA201
AXIAL0.4

RA101
AXIAL0.4

RJ303
AXIAL0.4

J10AC
BLOCK4

J9VS
BLOCK4

RJ204
AXIAL0.4

U8P
TO-220

U9N
TO-220

C803A
RAD0.2

C316
RAD0.2

C501
RAD0.2

R505
AXIAL0.4

R502
AXIAL0.4

R506
AXIAL0.4

R509
AXIAL0.4

R501
AXIAL0.4

D317
DIODE0.4

D301
DIODE0.4

D311
DIODE0.4

C702
RAD0.2

C317
RAD0.2

C302
RAD0.2

C311
RAD0.2

C301
RAD0.2

C313
RAD0.2

R301
AXIAL0.4

R318
AXIAL0.4

R316A
AXIAL0.4

R316B
AXIAL0.4

R702
AXIAL0.4

R704
AXIAL0.4

R313G
AXIAL0.4

R511Q
AXIAL0.4

D902B
DIODE0.4

D801B
DIODE0.4

D902A
DIODE0.4

D801A
DIODE0.4

U1
DIP14
LF347

U5
DIP14
4071

U2
DIP14
LM324

U7
DIP8
LM311

U3
DIP18
UC3637

C604
RAD0.2

C608
RAD0.2

C204
RAD0.2

C211
RAD0.2

C104
RAD0.2

C111
RAD0.2

C306
RAD0.2

C704
RAD0.2

C708
RAD0.2

C514
RAD0.2

C305
RAD0.2

R212
AXIAL0.4

R210
AXIAL0.4

R205
AXIAL0.4

R203
AXIAL0.4

C205
RAD0.2

C212
RAD0.2

C210
RAD0.2

C203
RAD0.2

R110
AXIAL0.4

R113B
AXIAL0.4

R101
AXIAL0.4

R102A
AXIAL0.4

R313
AXIAL0.4

R106
AXIAL0.4

R113C
AXIAL0.4

R102B
AXIAL0.4

R109
AXIAL0.4

R110G
AXIAL0.4

R108
AXIAL0.4

R114
AXIAL0.4

R112G
AXIAL0.4

D106
DIODE0.4

D107
DIODE0.4

C107
RAD0.2

R606
AXIAL0.4

R112
AXIAL0.4

C903B
RB.2/.4

C803B
RB.2/.4

C801
RB.3/.6

C902
RB.3/.6

C903A
RAD0.2

R607
AXIAL0.4

R603H
AXIAL0.4

R603
AXIAL0.4

U6
DIP8

C603
RAD0.2

A2VO
AD215

J2FP
DB15RA/
M

R504
AXIAL0.4

R503
AXIAL0.4

RQ2J2
AXIAL0.4

RQ3J2
AXIAL0.4

J1CS
DB15RA/F

A1VI
AD215

J3DR
IDC14

J4DR
BNC2

SW1
DIP8

J5VO
BNC2

J6VI
BNC2

J7IO
BNC2

J8IL
BNC2

R114Z
AXIAL0.3

R113
AXIAL0.5

2. PCB Net List

NET1
Q3-C
RQ3J2-2

NET2
Q3-B
R504-2

NET3
Q2-C
RQ2J2-2

NET4
Q2-B
R503-2

NET5
Q1-C
R603-2
U6-3
C603-2

NET6
Q1-B
R511Q-1

NET7
R208Z-1
U2-9
U2-8
U3-12
R110-1

NET8
R208Z-2
J8IL-1

NET9
DA201-A
RA201-2
J9VS-2
A2VO-2

NET10
DA201-K
RA201-1
J9VS-1
A2VO-1

NET11
DA101-A
RA101-2
J9VS-4
A1VI-2

NET12
DA101-K
RA101-1
J9VS-3
A1VI-1

NET13
RJ303-1
J3DR-3

NET14
RJ303-2
RJ204-2
U8P-O
C803A-1
C501-2
R506-2
R301-1
U1-4
U5-14
U2-4
U7-8
U3-6
C608-1
C204-1
C104-1
C306-2
C708-2
C514-1
R313-1
C803B-P
R603H-1
U6-8
A2VO-42
J2FP-12
J2FP-11
J2FP-3
J1CS-11
J1CS-3
A1VI-42
J3DR-9
J3DR-8

NET15
J10AC-1
D902A-K
D801A-A

NET16
J10AC-4
D902B-K
D801B-A

NET17
RJ204-1
J2FP-4

NET18
U8P-I
D801B-K
D801A-K
C801-P

NET19
U9N-O
C316-2
R318-2
R316A-2
R704-1
U1-11
U2-11
U7-4
U3-5
C604-2
C211-2
C111-2
C704-2
C305-2
C903B-N
C903A-1
U6-4
A2VO-44
J1CS-10
J1CS-2
A1VI-44

NET20
C501-1
R501-1
U5-1
J1CS-1

NET21
R505-2
U5-5
J2FP-15

NET22
R502-1
U5-2
J2FP-6

NET23
R506-1
U5-6
U7-7

NET24
R509-1
U5-9
U5-8

NET25
D317-A
C317-2
U7-3
U3-17

NET26
D317-K
C317-1
R316A-1
R316B-1
U3-16

NET27
D301-K
C301-2
R301-2
U3-1

NET28
D311-K
C311-2
U3-11
U3-9
R113-2

NET29
C702-2
R702-2
R704-2
U7-2

NET30
C302-2
U3-10
U3-8
U3-2

NET31
C313-1
R313G-1
U3-13
R313-2

NET32
R318-1
U3-18

NET33
R316B-2
U2-14
U2-13
R109-1
J7IO-1

NET34
R511Q-2
U5-11
U3-14
J3DR-4

NET35
U1-1
R101-2
R106-2
R112-1

NET36
U1-2
R101-1
R102A-2
R102B-2

NET37
U1-6
R106-1
D106-A
C107-1

NET38
U1-7
R113C-2
D107-A
C107-2

NET39
U1-8
R113B-2
R108-1

NET40
U1-9
R109-2
R108-2

NET41
U1-10
R110-2
R110G-1

NET42
U1-12
R112G-1
R112-2

NET43
U1-13
R113B-1
R113C-1
R114-1

NET44
U1-14
R114-2
R114Z-2

NET45
U5-13
U5-3
J2FP-7
R503-1

NET46
U5-12
U5-4
J2FP-8
R504-1

NET47
U2-12
R212-2
C212-2

NET48
U2-10
R210-2
C210-2

NET49
U2-7
U2-6
J6VI-1

NET50
U2-5
R205-2
C205-1

NET51
U2-3
R203-2
C203-2

NET52
U2-2
U2-1
R102A-1
J5VO-1

NET53
U3-4
SW1-23A

NET54
R212-1
J1CS-4

NET55
R210-1
J1CS-5

NET56
R205-1
A1VI-38

NET57
R203-1
A2VO-38

NET58
R102B-1
R607-1
U6-7

NET59
D106-K
D107-K

NET60
R606-2
U6-2
U6-1

NET61
R606-1
R607-2
U6-6

NET62
R603H-2
J2FP-9

NET63
R603-1
J2FP-10

NET64
A2VO-4
A2VO-3

NET65
J2FP-14
RQ3J2-1

NET66
J2FP-5
RQ2J2-1

NET67
A1VI-4
A1VI-3

NET68
J3DR-2
SW1-23B
SW1-1B

NET69
J4DR-1
SW1-1A
SW1-2A

NET70
SW1-3B
SW1-2B
R113-1

NET71
SW1-3A
R114Z-1

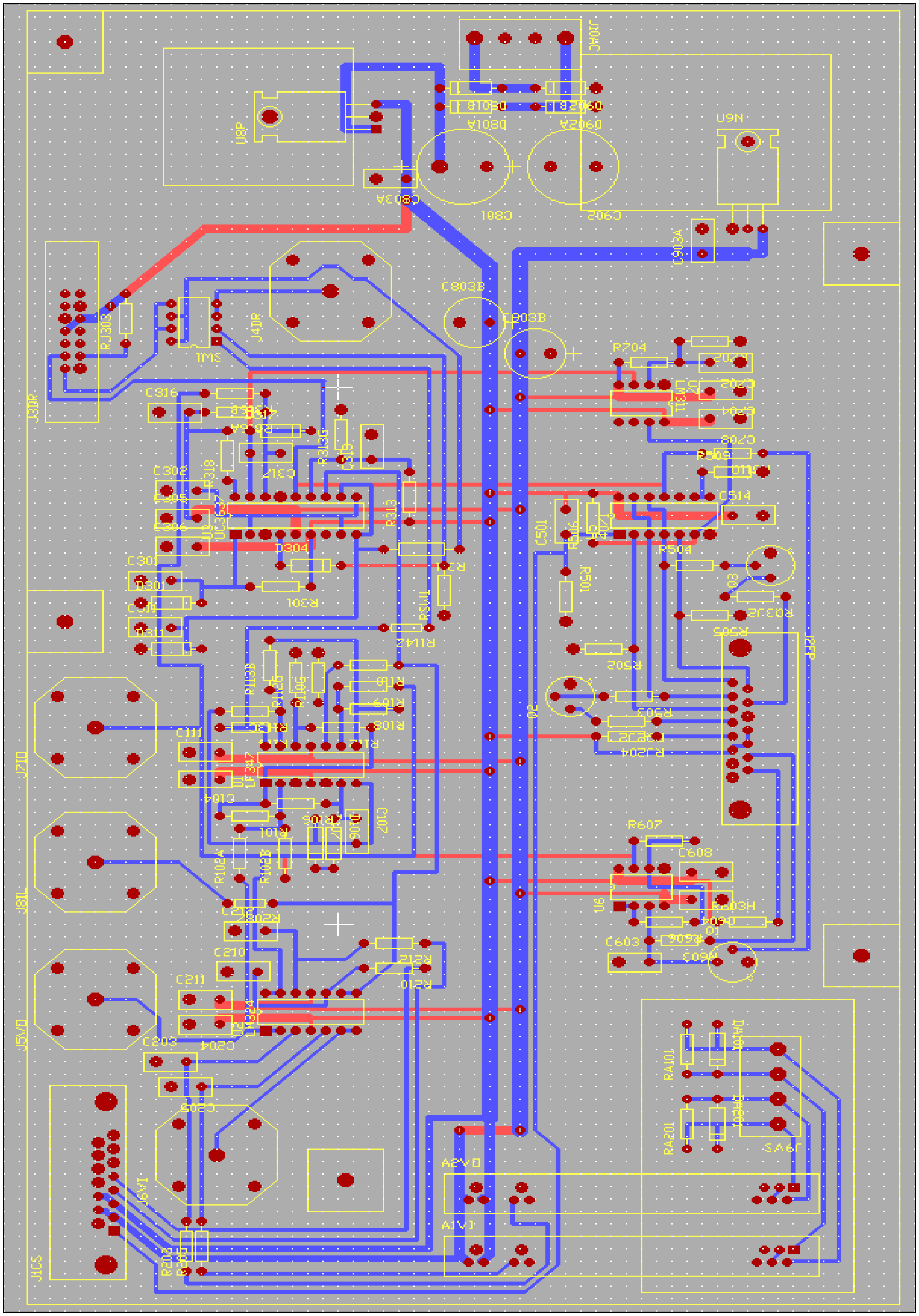

Figure D-1, PCB Layout.

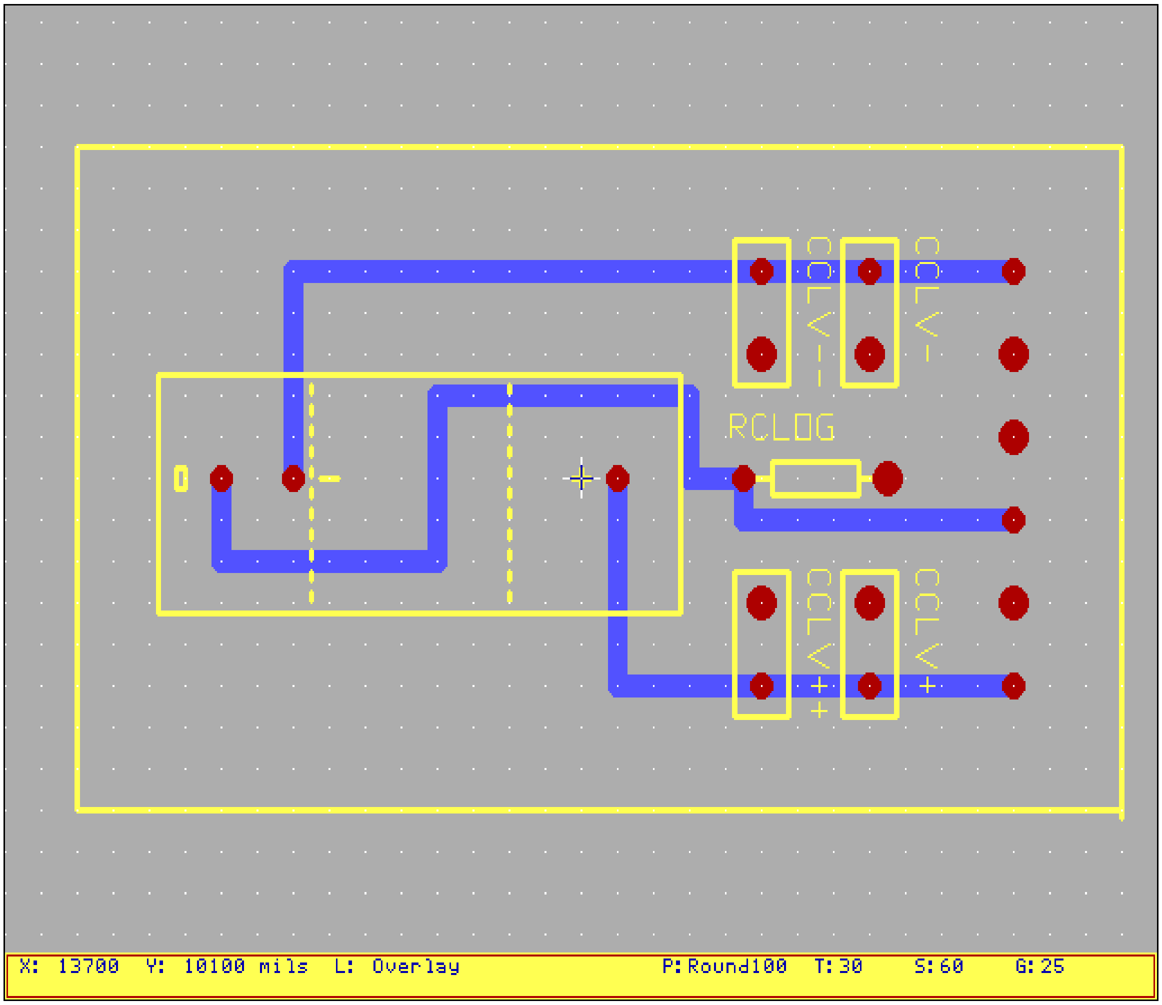

Figure D-2, Current Sensor Board Overlay.

APPENDIX E. dSPACE PROCEDURES

The SIMULINK model is created first, using the general math blocks from the SIMULINK library. Each functional block will be discussed. The following figure shows the software-only simulation structure.

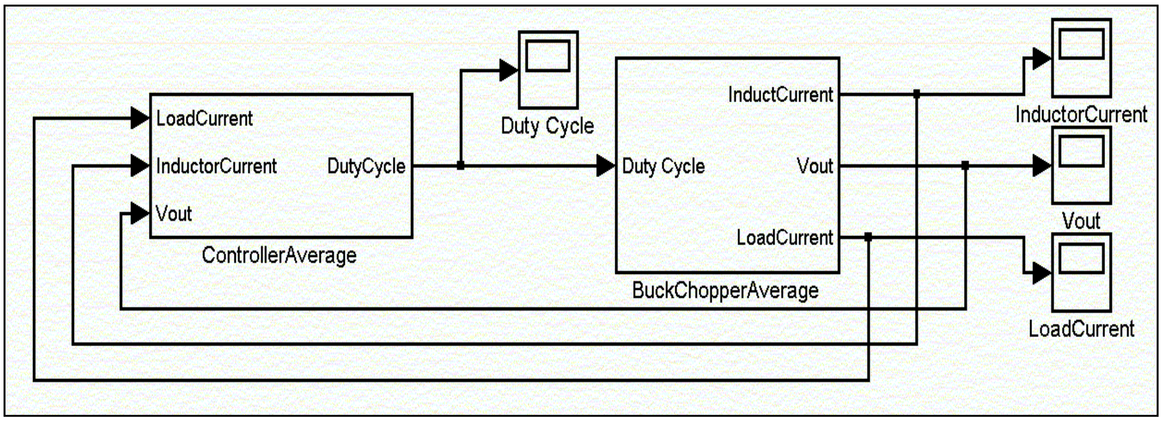

Figure E-1.

The *Controller Average* and *BuckChopperAverage* subsystem blocks have been uniquely derived and can be found in the SIMULINK *signals and systems* library. Double-clicking on the subsystem block exposes its contents. The following figure displays the *Controller Average* subsystem.

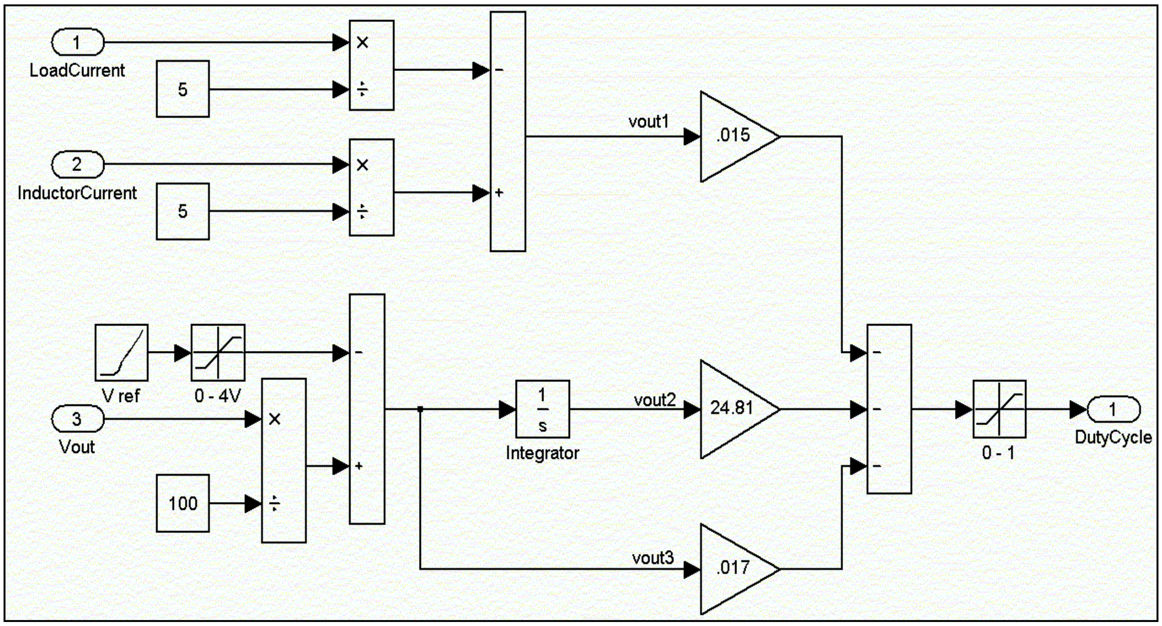

Figure E-2.

The input and output bubbles are found in the SIMULINK *signals and systems* library. They are used to create the higher-level input and output connections. The contents of the *BuckChopperAverage* subsystem are shown below.

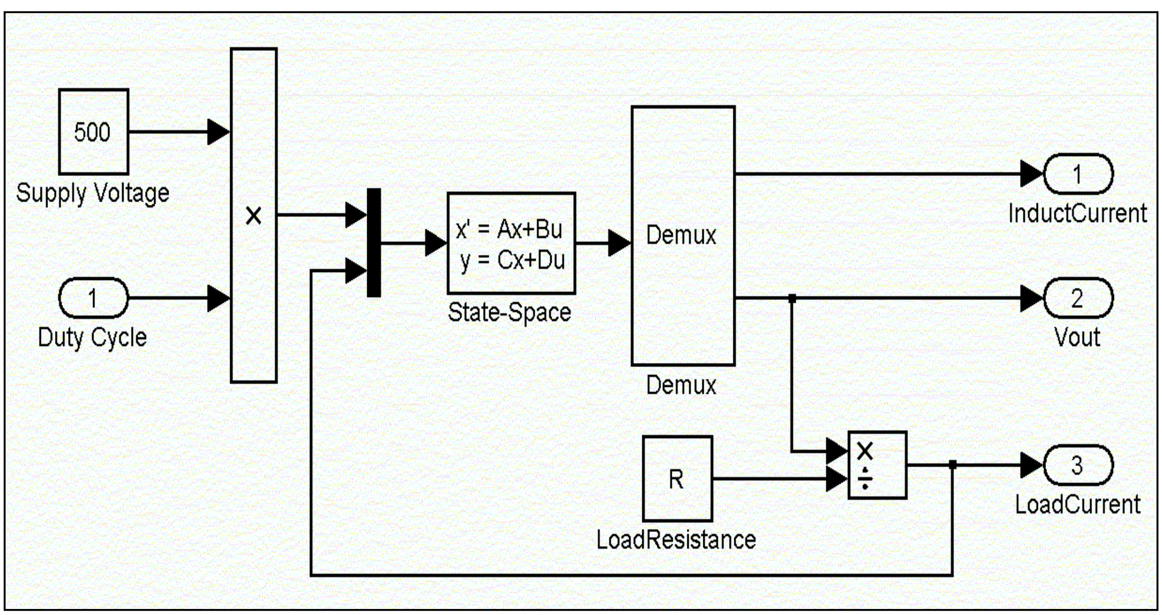

Figure E-3.

This is the state-space-averaged mathematical model for the buck chopper and utilizes the averaged inductor current and the averaged output capacitor voltage as state variables. The following figure shows the same system with a dSPACE PWM output block found in the SIMULINK dSPACE library.

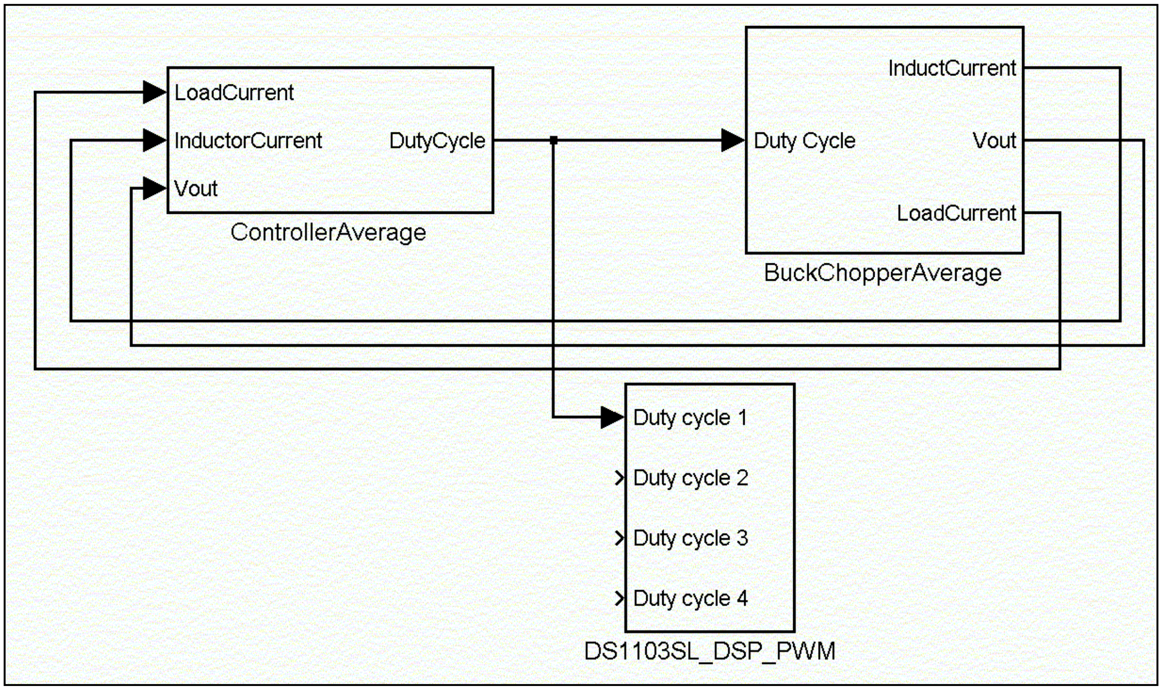

Figure E-4.

This model allows the evaluation of the PWM output waveform without connecting hardware. For further interfacing, the following models were created to connect hardware and software models in dSPACE.

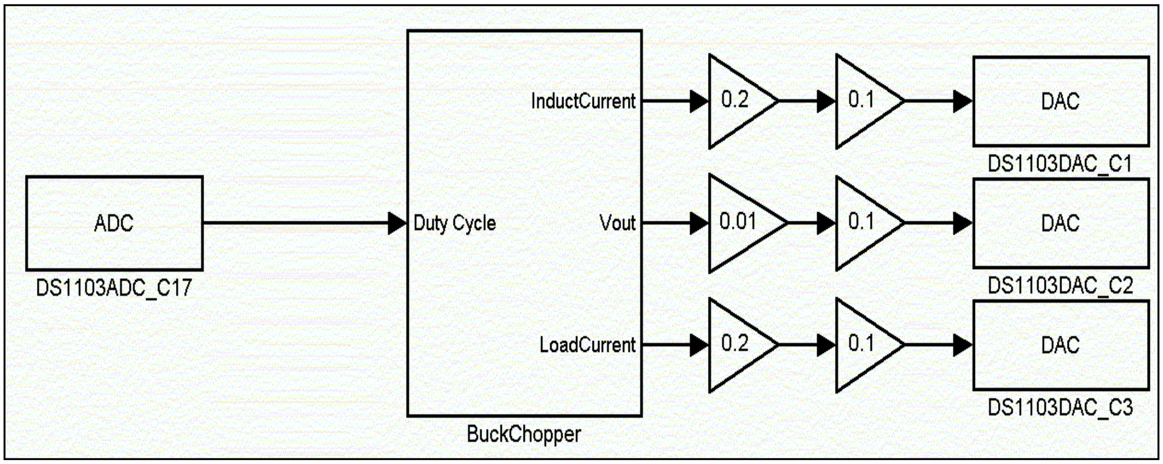

Figure E-5.

The ADC and DAC blocks are found in the SIMULINK dSPACE library. The input ADC can accept a signal ranging from 0 to 10 volts from the hardware controller. The dSPACE ADC will automatically scale the signal by 0.1. Since a 0 to 1 volt input is required for the duty cycle, an additional scaling gain was not required. On the output, the dSPACE ADC automatically scales the signal by 10.0. Hence, a 0.10 gain block was added to each output to maintain proper scaling. The other gain scaling blocks are due to the actual model. The numbers on each of the ADC/DAC blocks correspond to the dSPACE i/o board. The C17 corresponds to ADCH17. The C1, C2, and C3 refer to DACH1, 2, and 3, respectively. [see Reference Manual page 91]

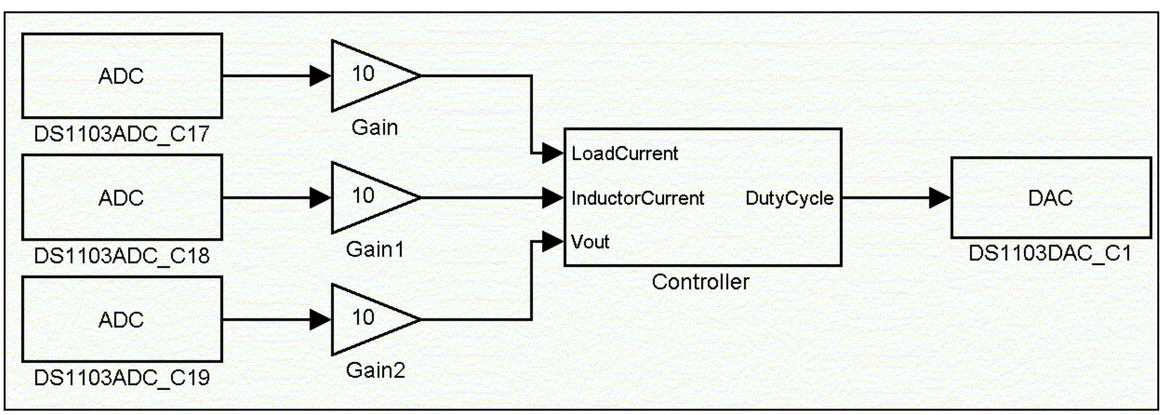

Figure E-6.

This model connects a hardware buck chopper to a software controller. The output from the software is a duty cycle to be fed into a PWM chip, which is then fed into the hardware buck chopper.

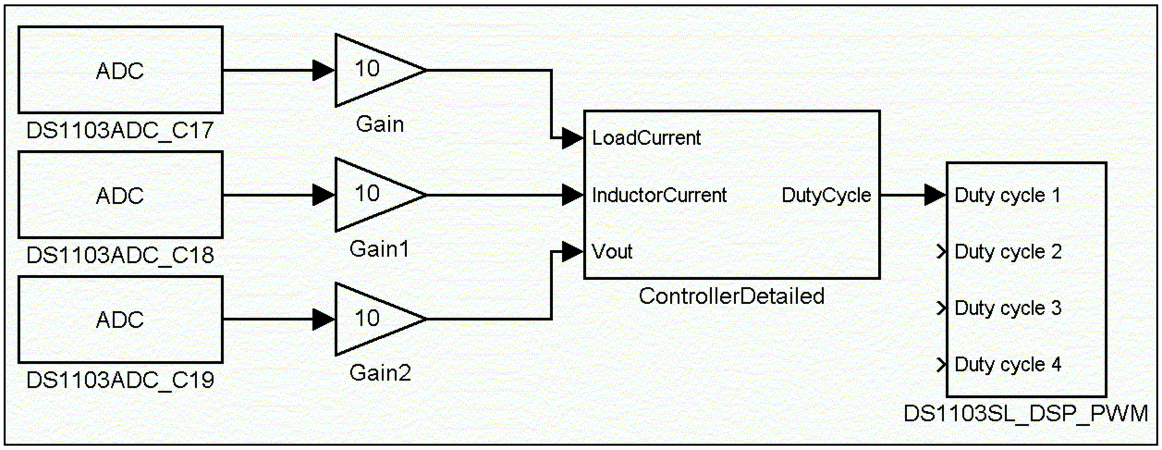

Figure E-7.

The model above only differs from the previous model in that the PWM signal is generated in software as opposed to hardware. As a result, the output from this model is a PWM waveform.

Once the model was built in SIMULINK, it was necessary to transform the model into a dSPACE readable file. First the component values (used in all previous models) were entered in the MATLAB command window, as shown below.

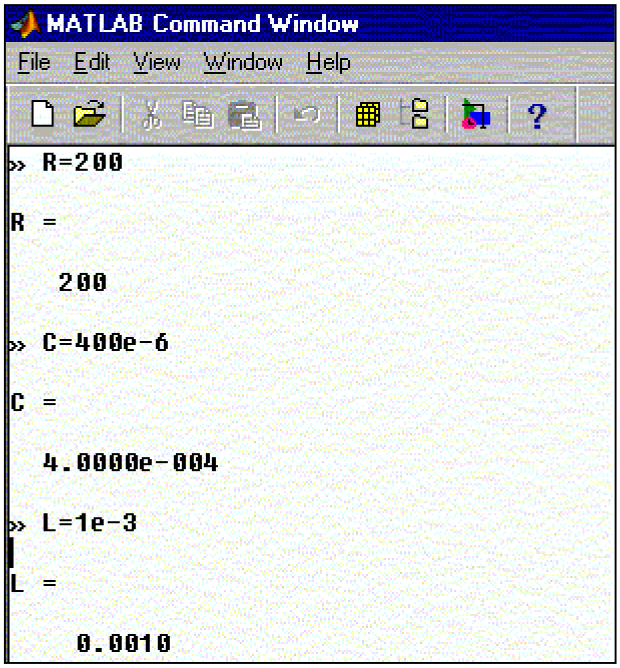

Figure E-8.

The next step was to compile the model in SIMULINK. The following figures show the menu options used to compile the SIMULINK model.

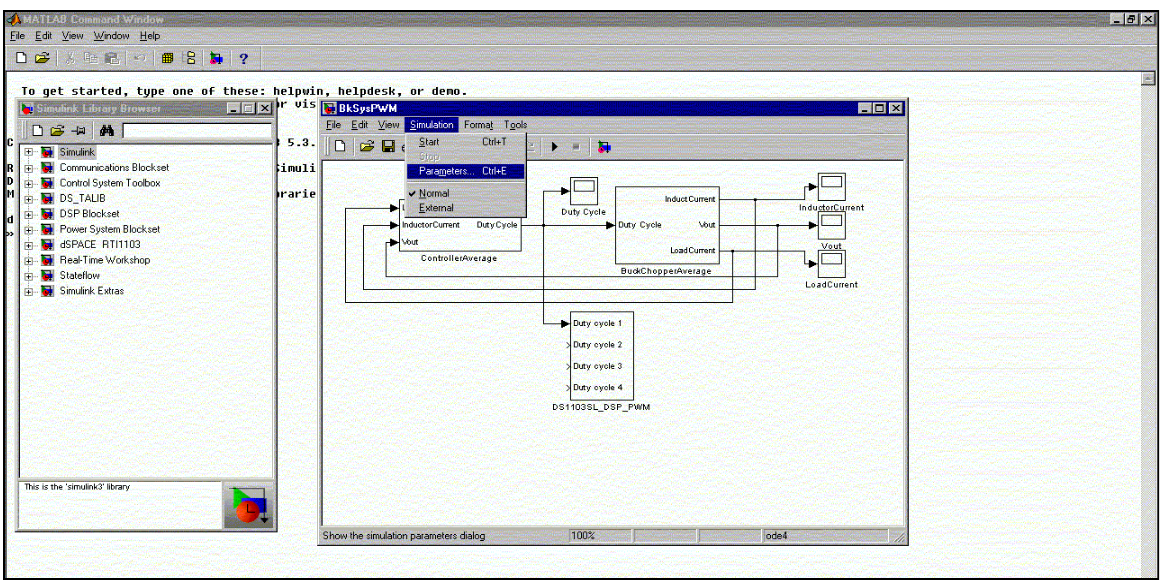

Figure E-9.

The first step is to select the *simulation* menu and open the *parameters* option. This brings up the following figure.

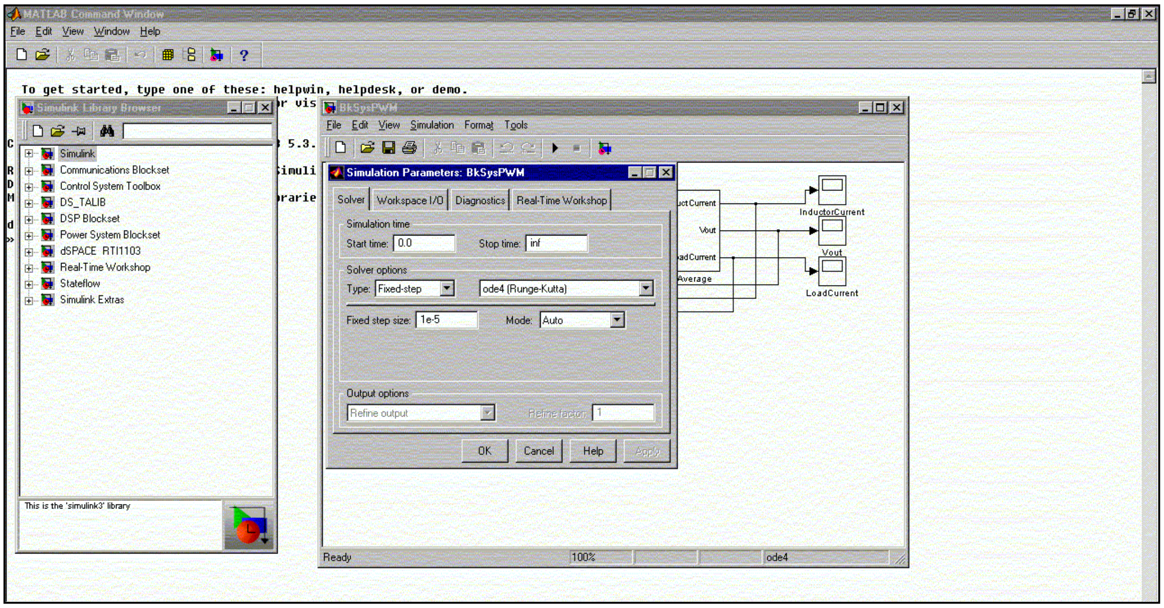

Figure E-10.

At this point the user can enter the simulation parameters. A time step of 1e-5 was selected (smaller values were not possible) and the Runge-Kutta Fixed-step algorithm employed. Next the *real-time workshop* tab is selected. The following figure is displayed.

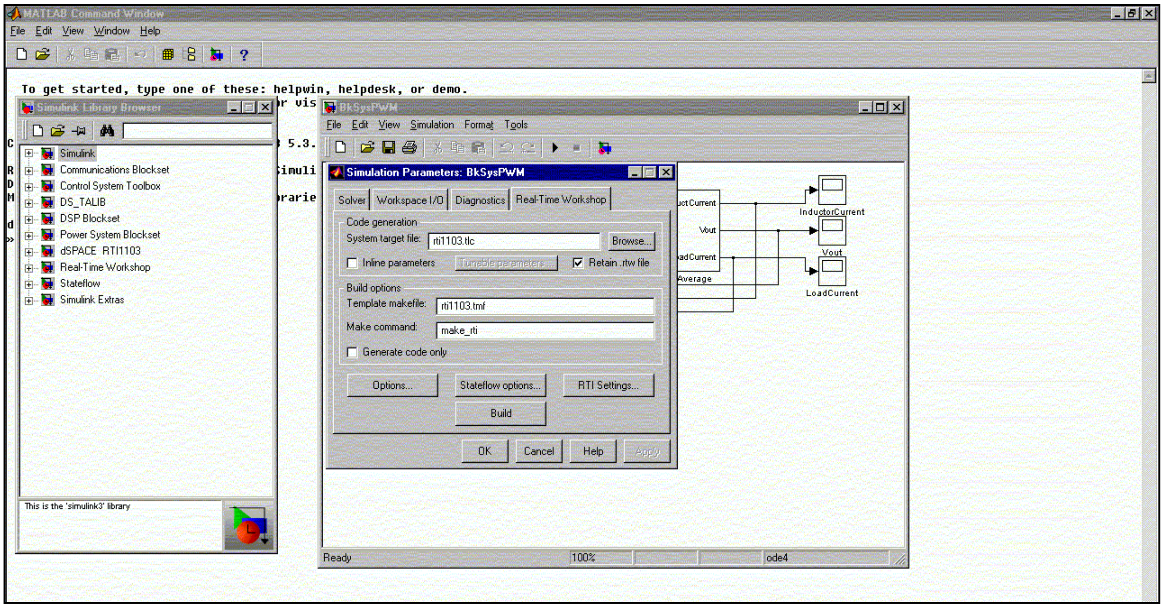

Figure E-11

The next step is to compile the SIMULINK model. In this step rti1103.tlc is entered for the target file, rti1103.tmt is entered for the template make file, and make_rti for the make command. The next step is to click the build button, bringing up the screen contained in the figure on the following page. This screen shows the results of the build process.

```
MATLAB Command Window
File  Edit  View  Window  Help

» R=200

R =

   200

» C=400e-6

C =

  4.0000e-004

» L=1e-3

L =

    0.0010

»
*** Starting RTI build procedure with RTI1103 3.4.1 (08-Sep-1999)


### Starting Real-Time Workshop build procedure for model: BkSysPWM
Warning: Input port 2 of block 'BkSysPWM/DS1103SL_DSP_PWM' is not connected.
Warning: Input port 3 of block 'BkSysPWM/DS1103SL_DSP_PWM' is not connected.
Warning: Input port 4 of block 'BkSysPWM/DS1103SL_DSP_PWM' is not connected.
### Invoking Target Language Compiler on BkSysPWM.rtw
### BkSysPWM.mk which is generated from rti1103.tmf is up to date
### Building BkSysPWM: dsmake -f BkSysPWM.mk WORKINGBOARD=ds1103

BUILDING PROGRAM (Single Timer Task Mode)

BUILD DIRECTORY "C:\MATLABR11\work"

COMPILING BkSysPWM.c
COMPILING C:\dSPACE\matlab\rti1103\c\rti_sim_engine.c
COMPILING C:\MATLABR11\rtw\c\src\ode4.c
COMPILING C:\MATLABR11\rtw\c\src\rt_sim.c

BUILDING LIBRARY "BkSysPWM_lib.o04" ...
BUILDING LIBRARY FINISHED

LINKING PROGRAM ...
LINKING FINISHED

LOADING PROGRAM "BkSysPWM.ppc" ...
LOADING FINISHED

MAKE PROCESS SUCCEEDED

### Successful completion of Real-Time Workshop build procedure for model: BkSysPWM

*** Finished RTI build procedure for model BkSysPWM
```

Figure E-12.

Once the model has been built for dSPACE, it needs to be loaded into dSPACE. The following figure displays a dSPACE window once it has been opened.

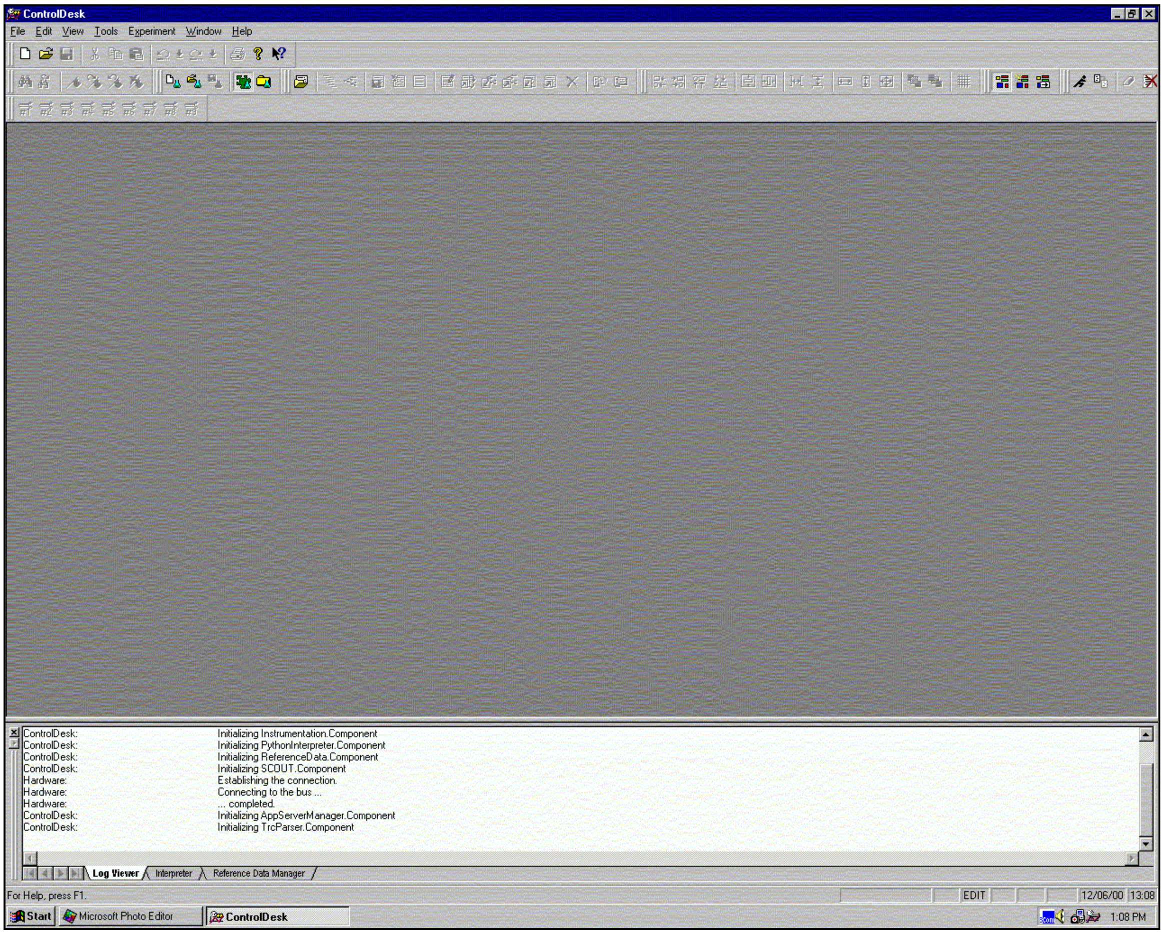

Figure E-13.

Once dSPACE is open, it is necessary to activate the *navigator*. The following figure shows that this command is located under the *view* menu.

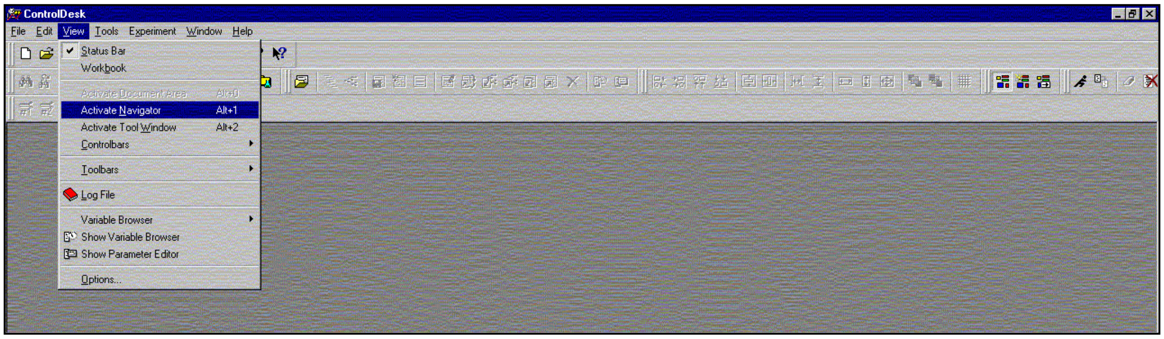

Figure E-14.

Once the *navigator* has been activated, it is necessary to click on the *Hardware* tab to find the file that was built from SIMULINK. The following figure shows the file highlighted (BKsyspwm.ppc).

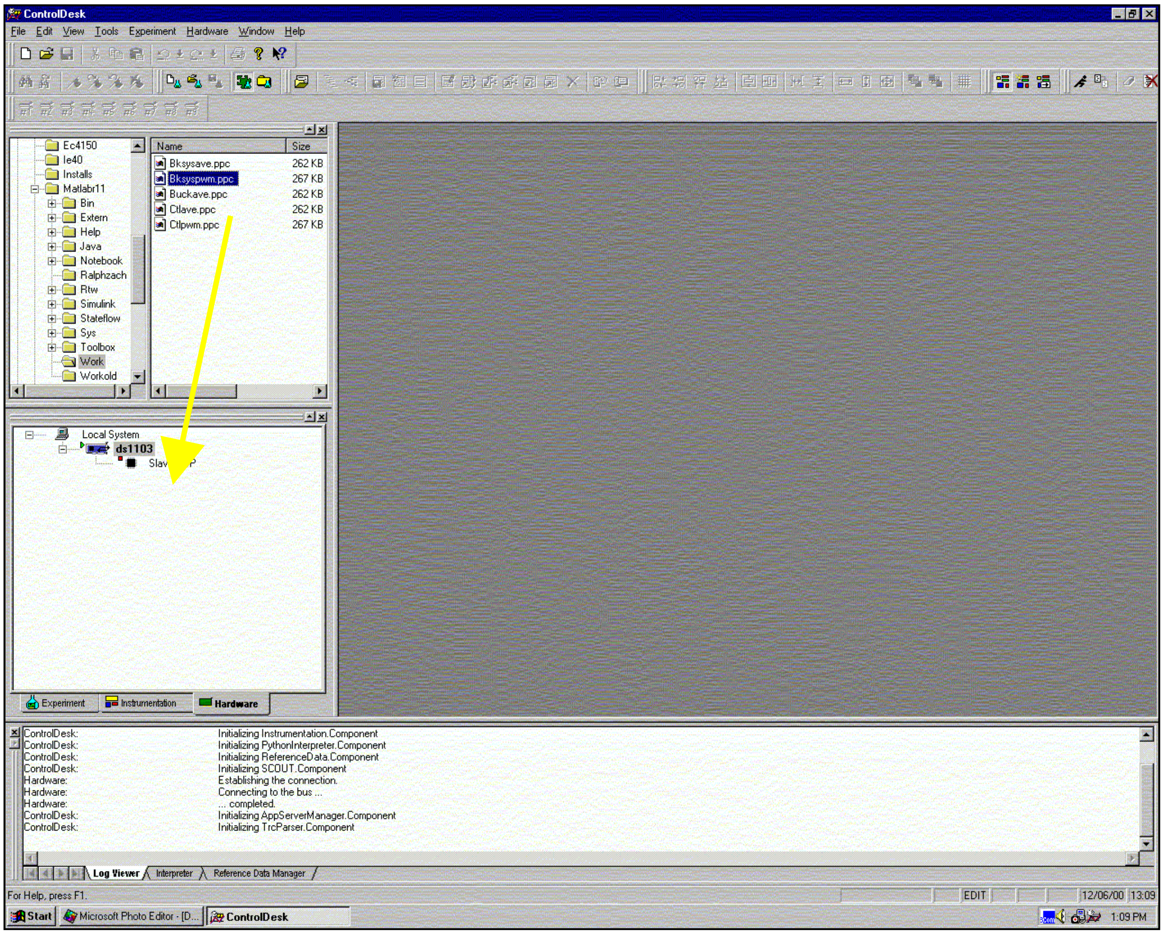

Figure E-15.

The file, which now has a .ppc extension on it, must be dragged to the ds1103 icon. The next figure is then displayed.

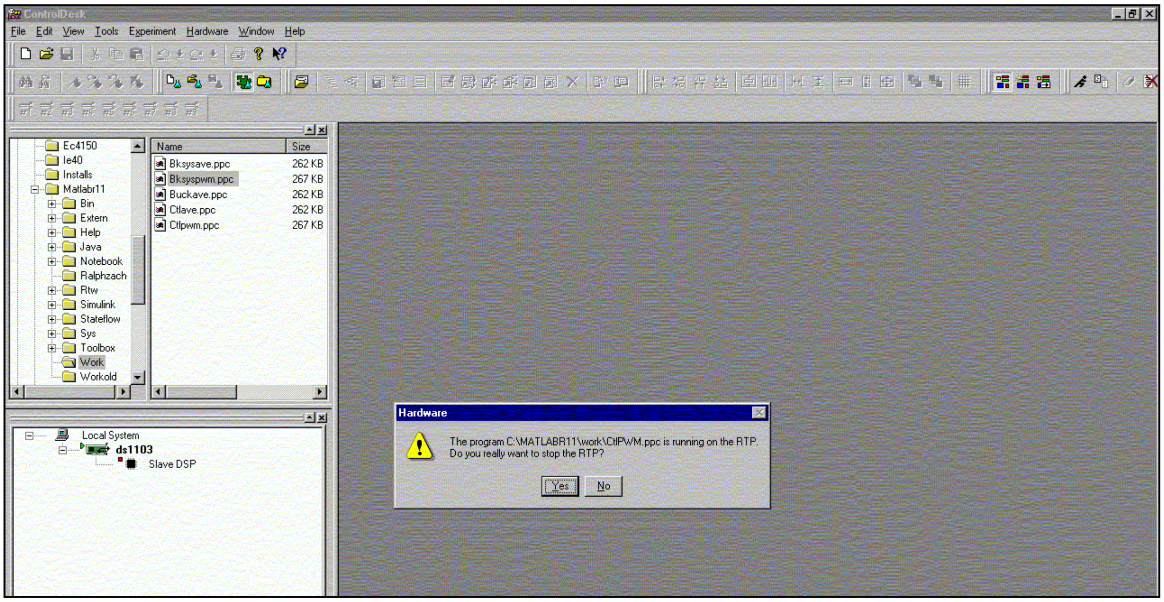

Figure E-16.

Answer this question by clicking *yes*. The following figure displays the next screen that comes up.

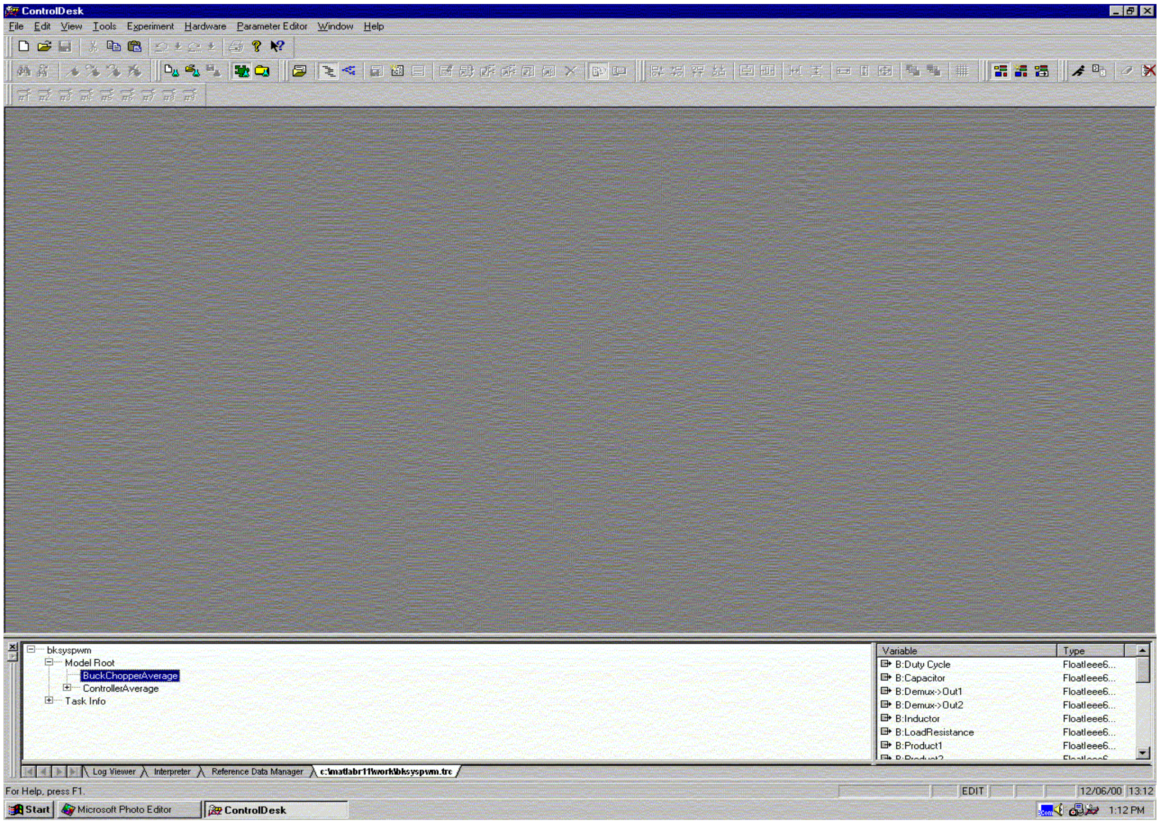

Figure E-17.

The *navigator* windows have been closed in this figure. The model that was built will be shown on the fourth tab at the bottom of the white space. At this point, it is time to either create a layout file or open an existing one. Initially the steps for opening an existing layout file will be documented. As the next figure shows, the first step to open an existing layout file is to go to the file menu and click *open*, then highlight *layout selection*. This will display a list of the layout files that have been created. The layout file called *BkChSys.lay* was then selected.

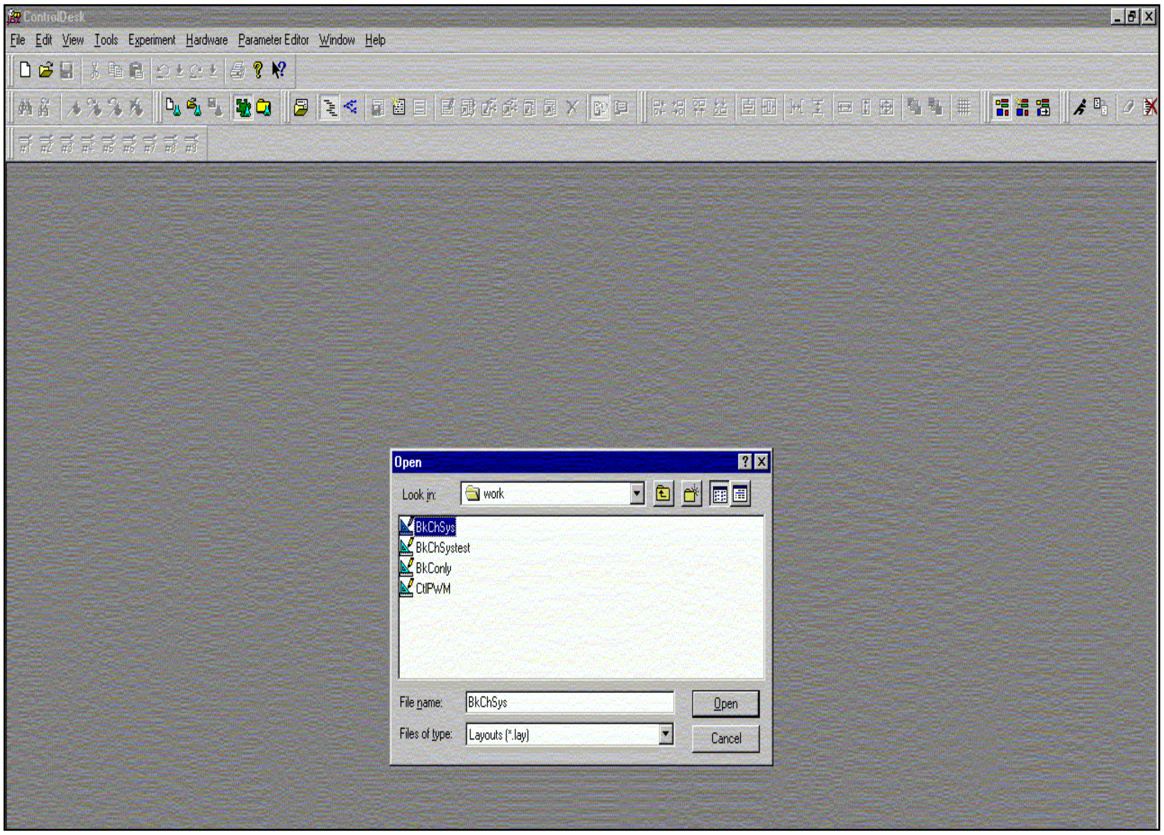

Figure E-18.

This file was opened and the following screen appeared.

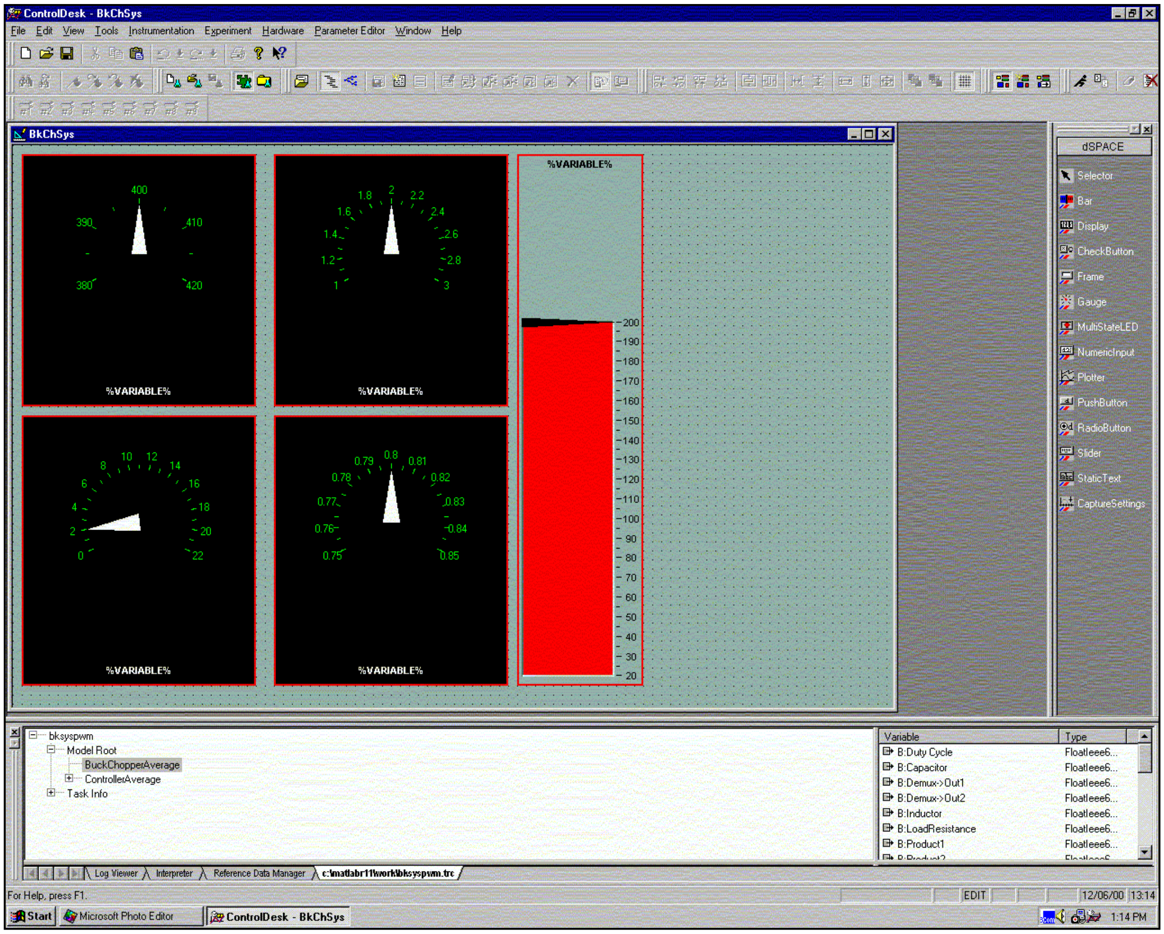

Figure E-19.

This layout screen shows four gauges and a slider. The gauges show specific outputs and the slider controls an input. In order to make a gauge or slider link to the model, it is necessary to drop the desired input/output onto the gauge or slider display. The following figure shows three gauges that have been linked to the model.

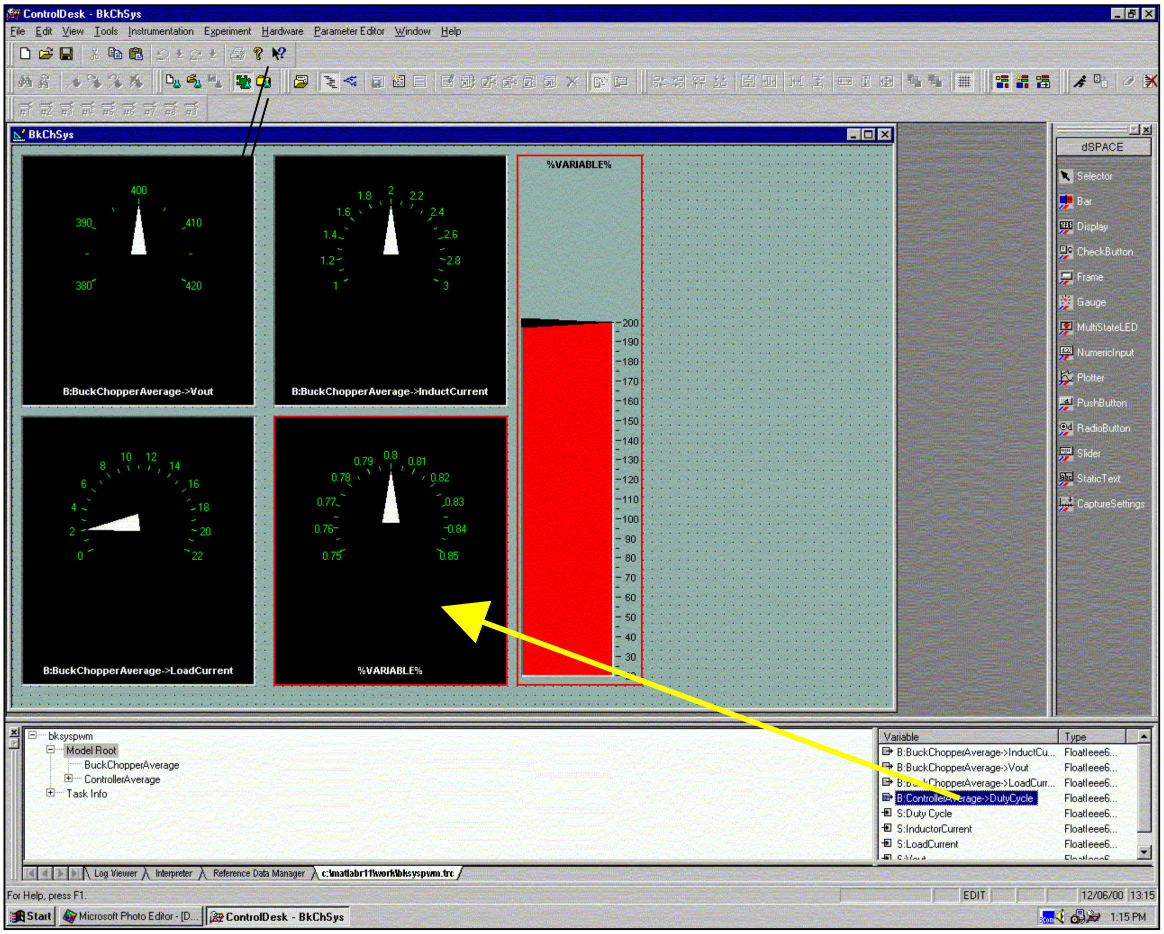

Figure E-20.

The fourth gauge will be linked once the highlighted duty cycle element is placed on the gauge itself. Once all the gauges and the slider are linked to the model, the screen will appear as it does in the following figure.

Now we are ready to activate the hardware connection. Once the i/o board is properly hooked up, the hardware connection needs to be refreshed. The following figure shows that under the hardware menu, select the *initialization* option, and then choose *refresh hardware connection.*

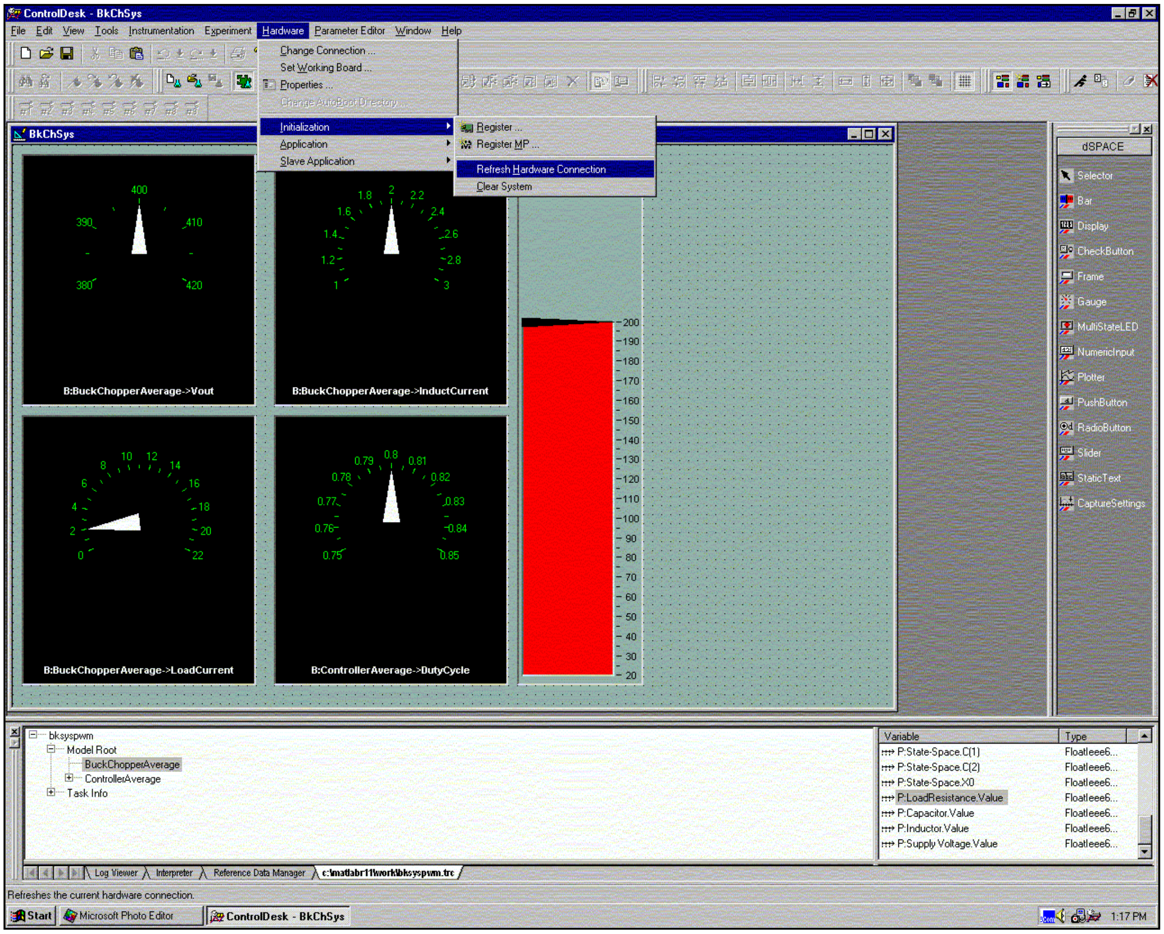

Figure E-21.

Next it is time to load the application. The following figure shows that the load command is under the *application* submenu of the *hardware* menu.

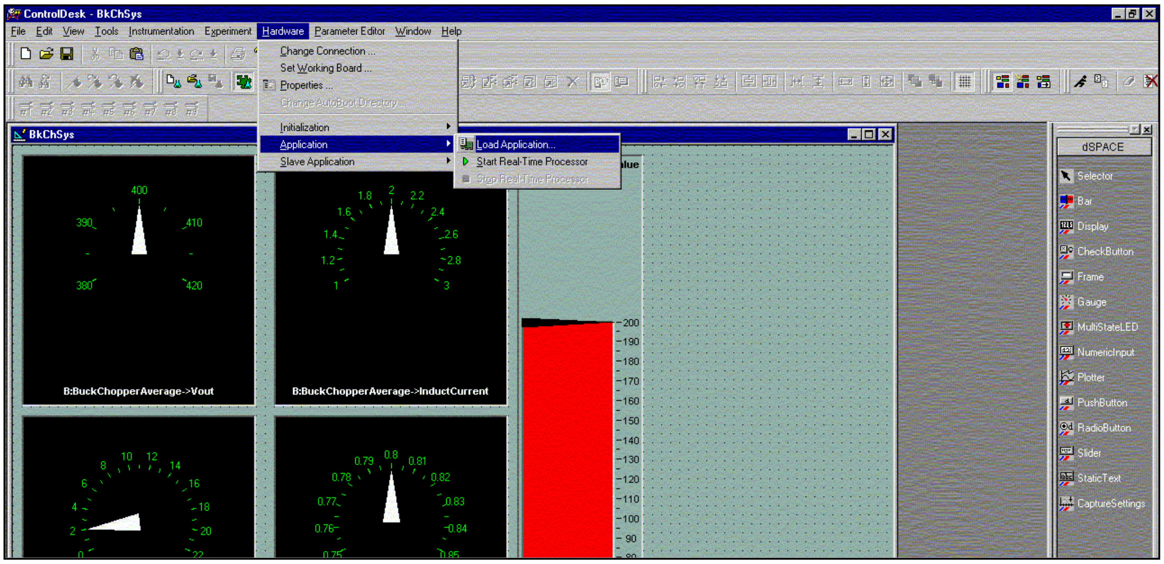

Figure E-22.

Once the *Load Application* has been selected, the following screen will appear as in the figure below.

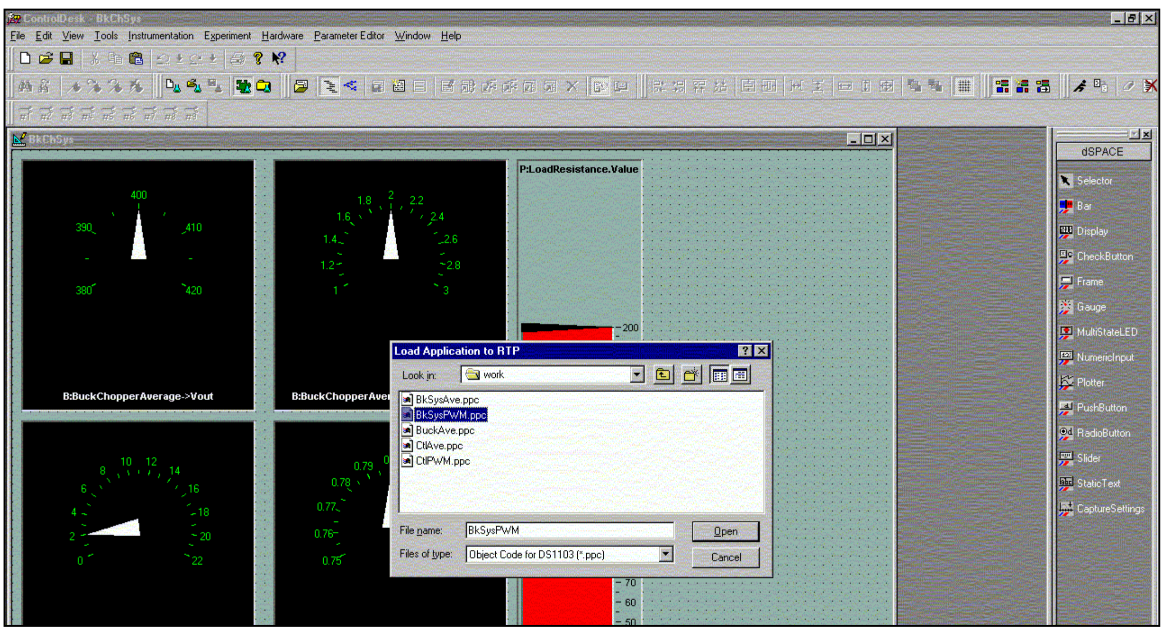

Figure E-23.

The *BkSysPWM.ppc* application is selected. Next, activate *animation mode*. This is located under the *instrumentation* menu as in the following figure.

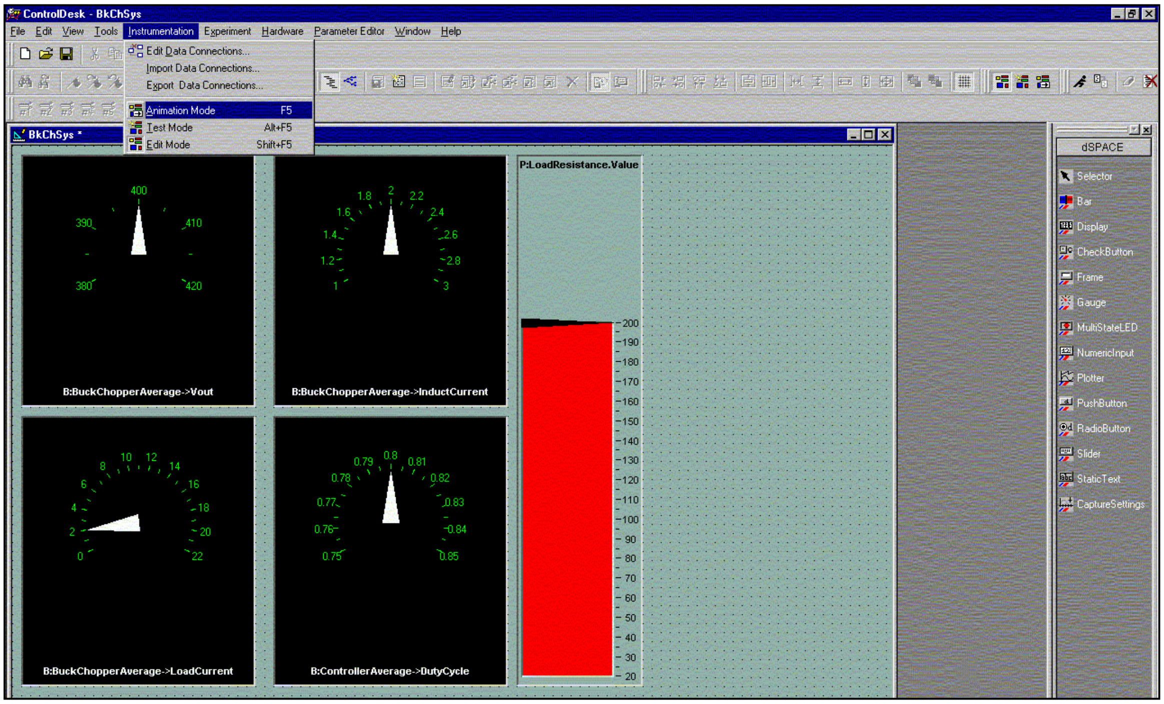

Figure E-24.

Once *animation* mode is selected, the hardware is energized. The following figure shows the activated control desk.

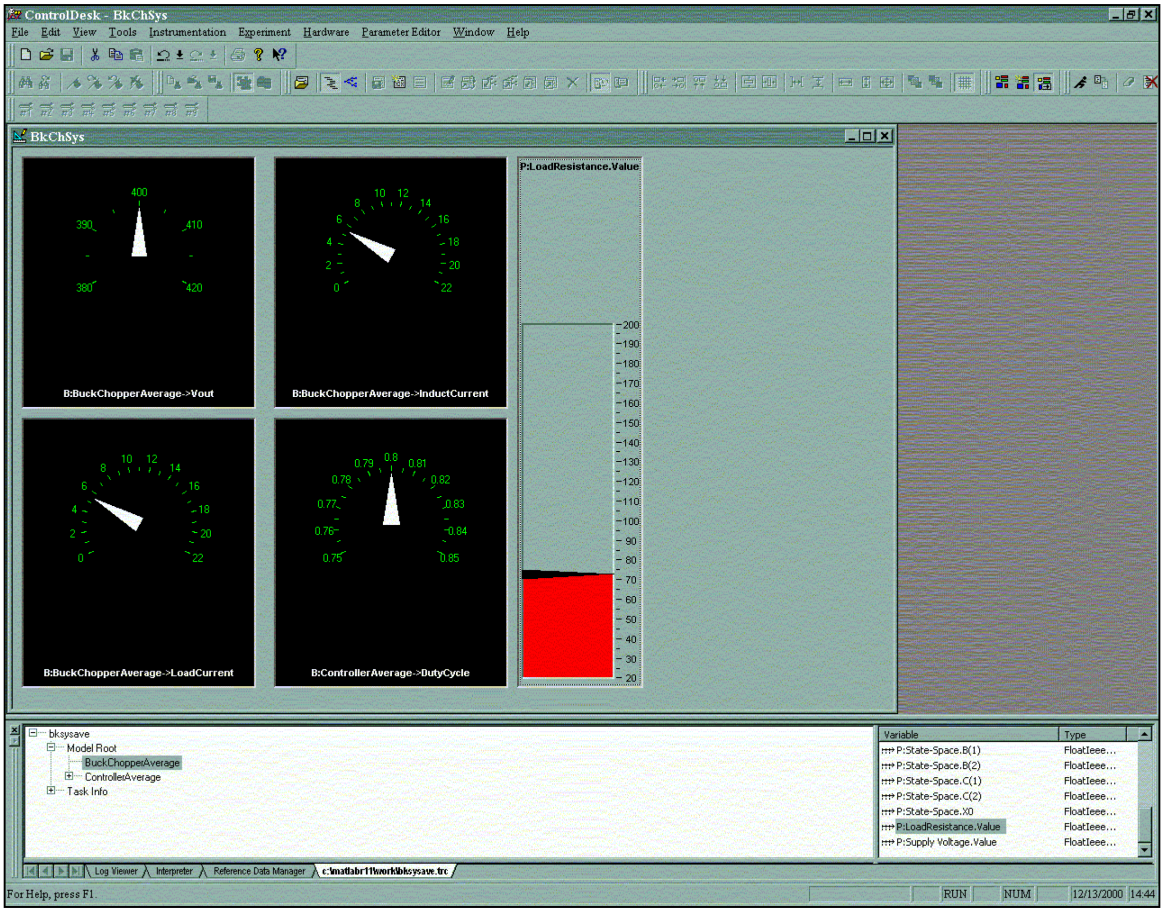

Figure E-25.

The above figure shows the slider at about 73. This corresponds to a load resistance of 73 Ohms. The duty cycle gauge is at 0.8, the output voltage gauge is at 400 Volts, the inductor current gauge is just over 5 Amps, and the load current is just over 5 Amps. From this screen the load resistance is adjusted real-time by moving the slider bar up and down.

Once a particular simulation is completed, it is necessary to deactivate the desktop and stop the real-time application. The following figure shows that the *edit mode* selection is under the *instrumentation* menu.

After *edit mode* has been selected, the *hardware* menu is accessed, the *application* submenu selected, and then the *stop real-time processor* tab is picked. The figure that follows the *edit mode* selection shows how the processor is disabled.

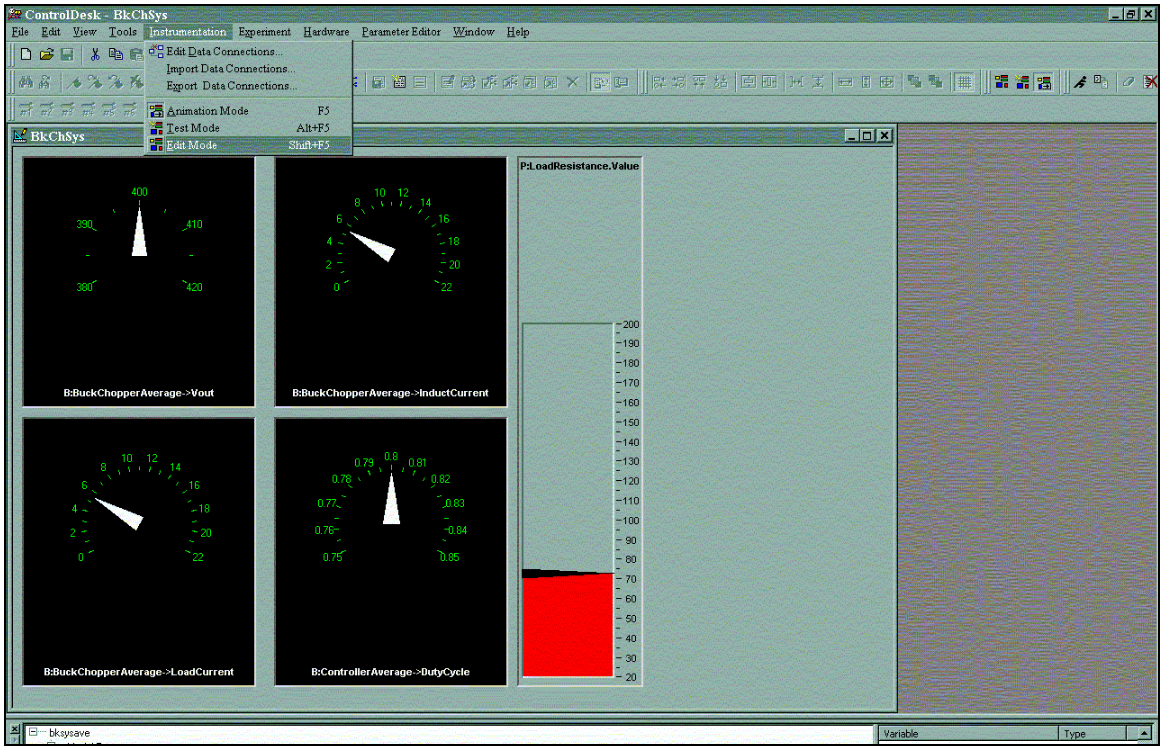

Figure E-26.

Above is *Edit Mode*. Below is *Stop Real Time Application*.

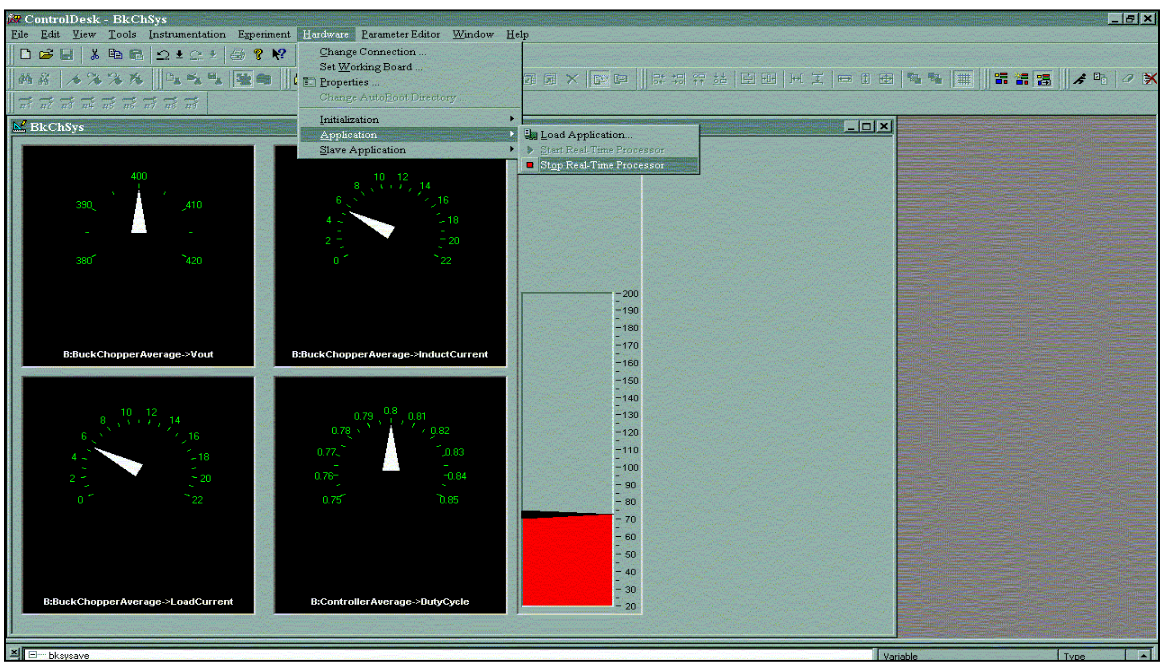

Figure E-27

The next set of figures show how to build a layout from scratch. The first step is to open a new file: select *layout* extension. The following figure shows the menu.

Figure E-28.

Once this has been selected, the screen in the following figure should appear.

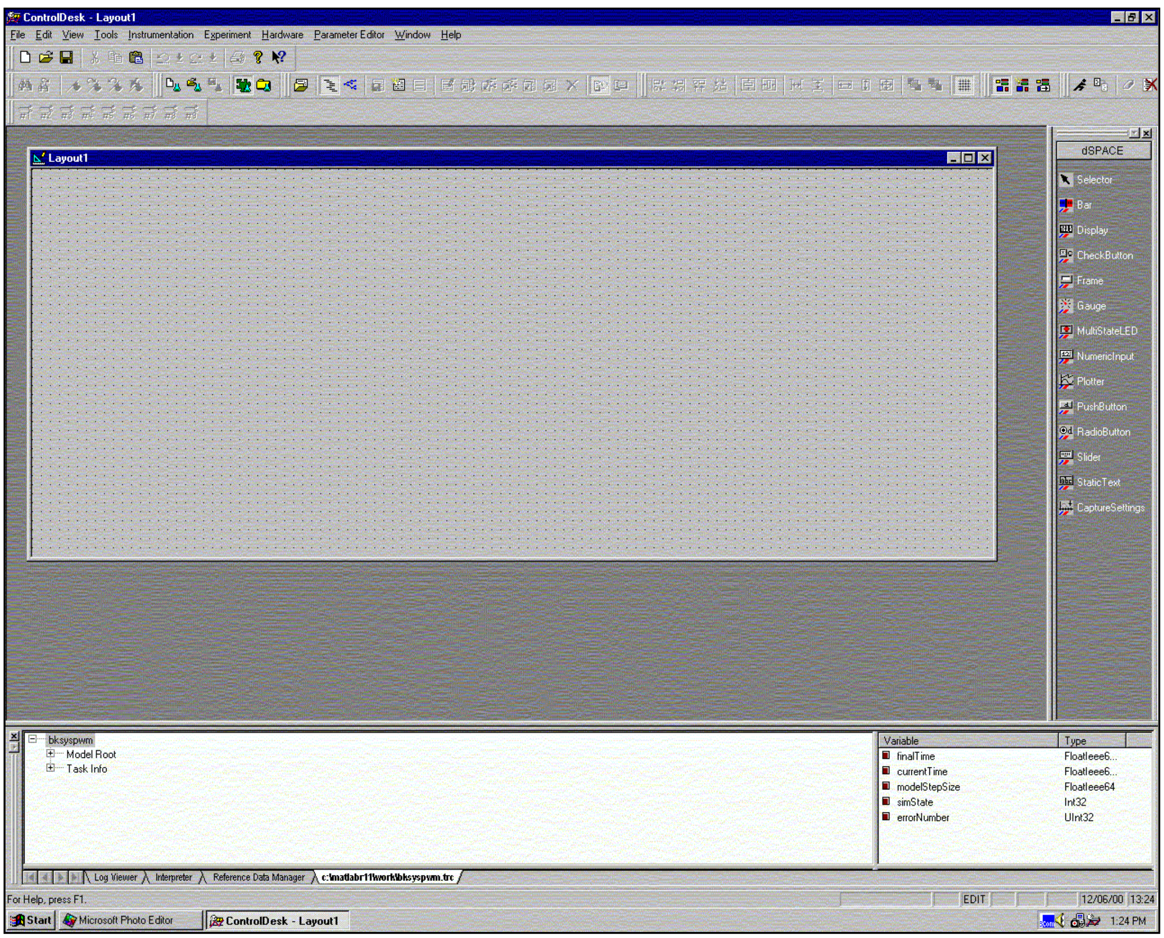

Figure 29.

Now it is time to select the control desk input and output displays. First select a gauge from the right side of the desktop. Double-click on the display desired, then move the cursor to the place on the desktop where the left top corner of the display is desired. Next, click the mouse button and then drag down and to the right to change the size of the display. The following figure shows a gauge that has been created in the above manner.

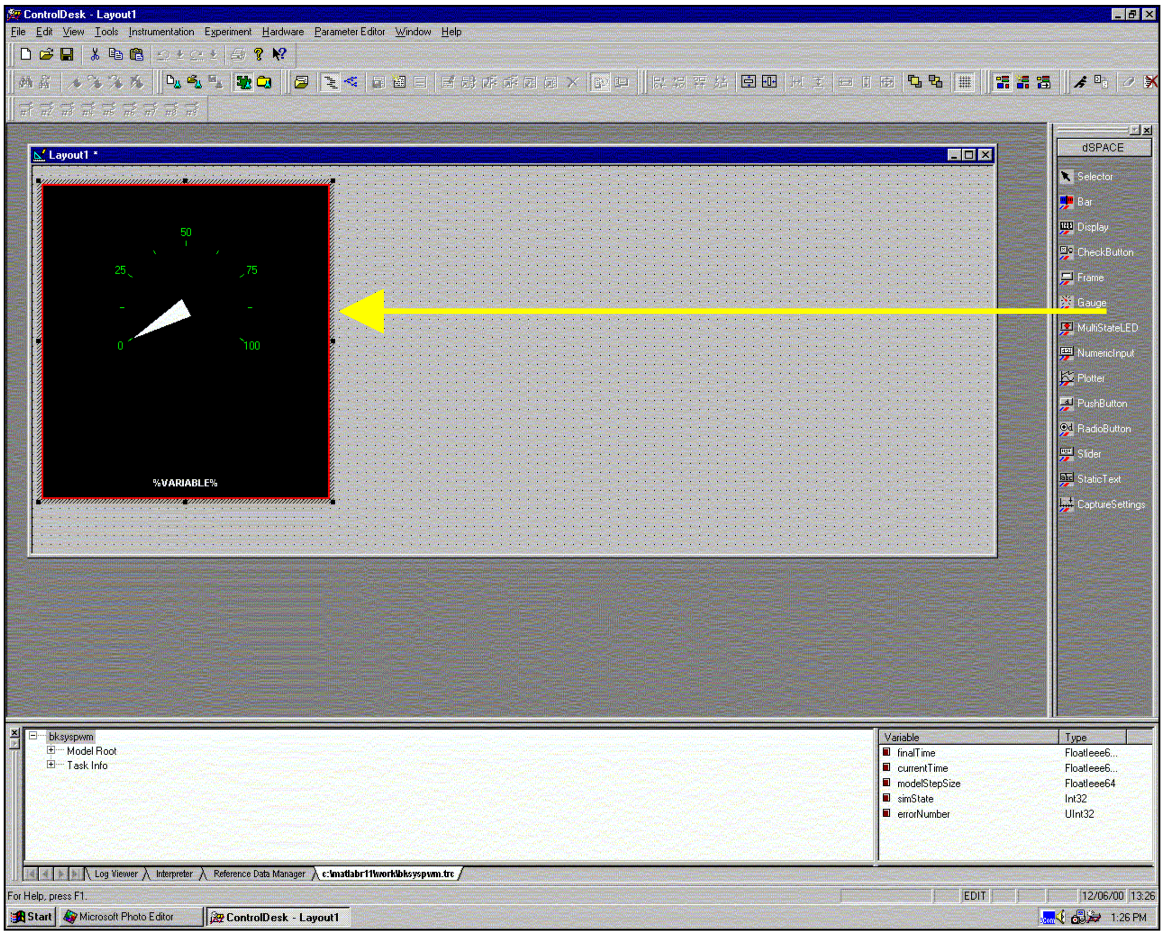

Figure E-30.

A slider may be added by following the same procedure as for the gauge. The following figure illustrates a slider.

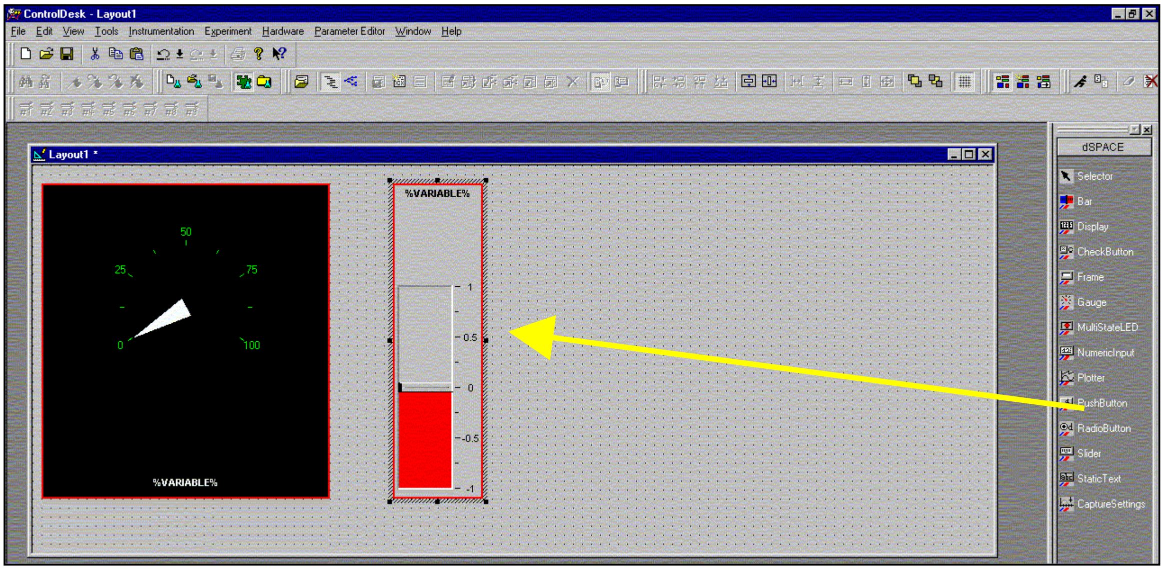

Figure E-31.

In order to change the display options for the slider gauge, the user must double click on the slider. The following figure illustrates the options that are displayed when the slider is double-clicked.

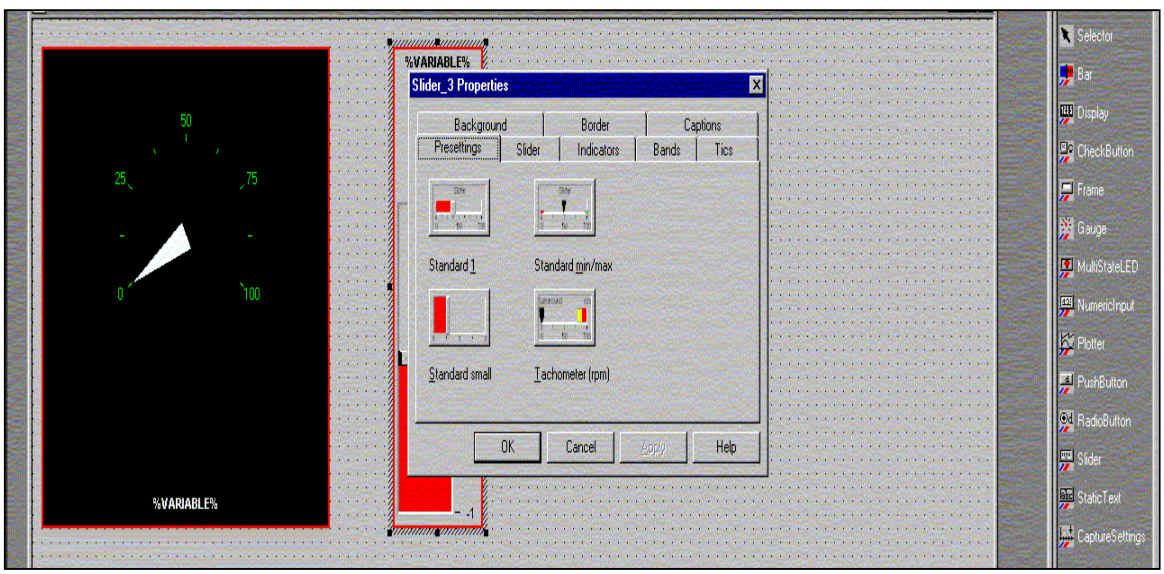

Figure E-32.

Upon the completion of dSPACE troubleshooting, the dSPACE model was executed with a hardware controller output load resistance of 200 ohms.

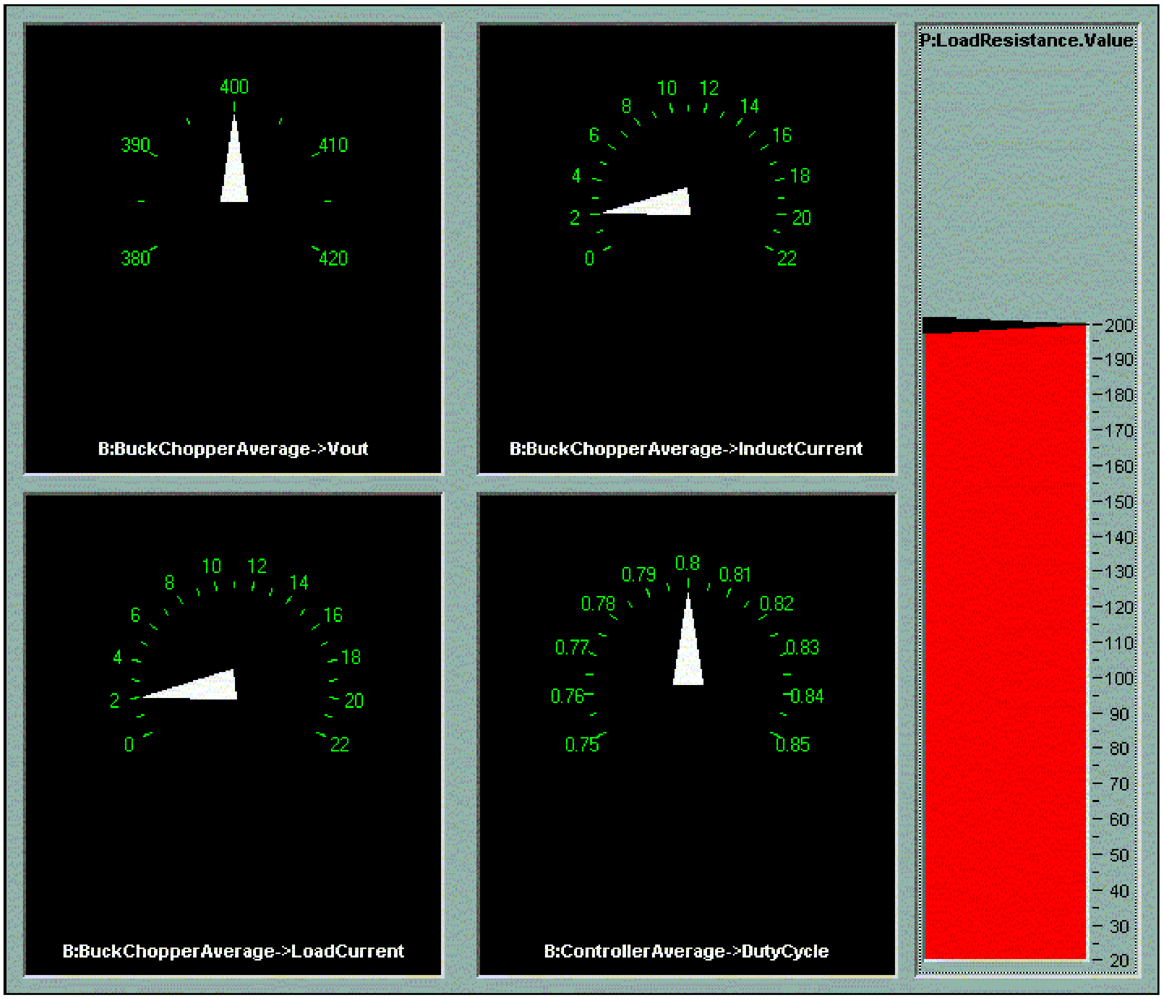

Figure E-33.

Next the load resistance was set to 20 Ohms and the model executed. The following figure shows the output on the dSPACE control desk.

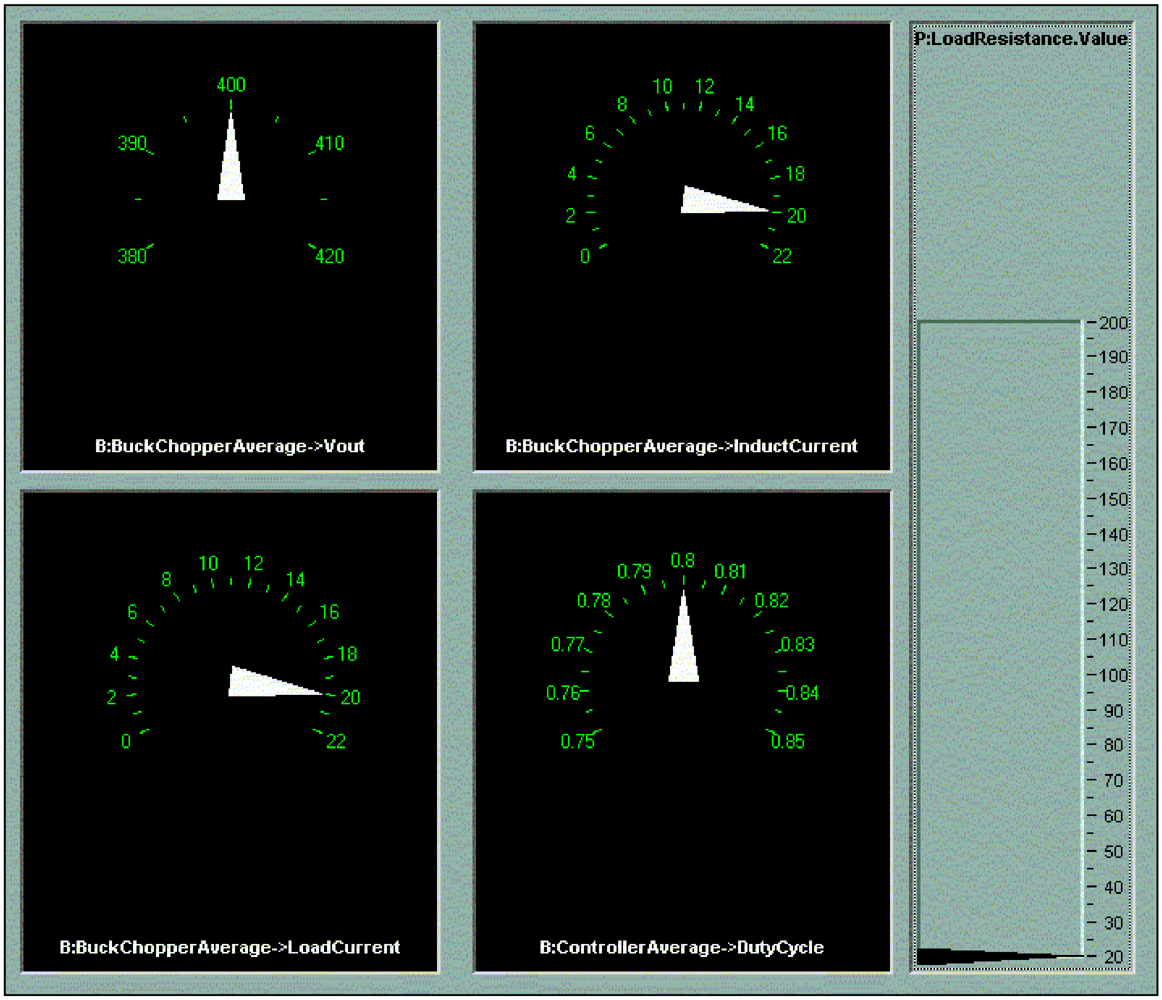

Figure E-34.

Finally, the resistance was set to 40 Ohms and the model executed. The figure on the following page shows the dSPACE results.

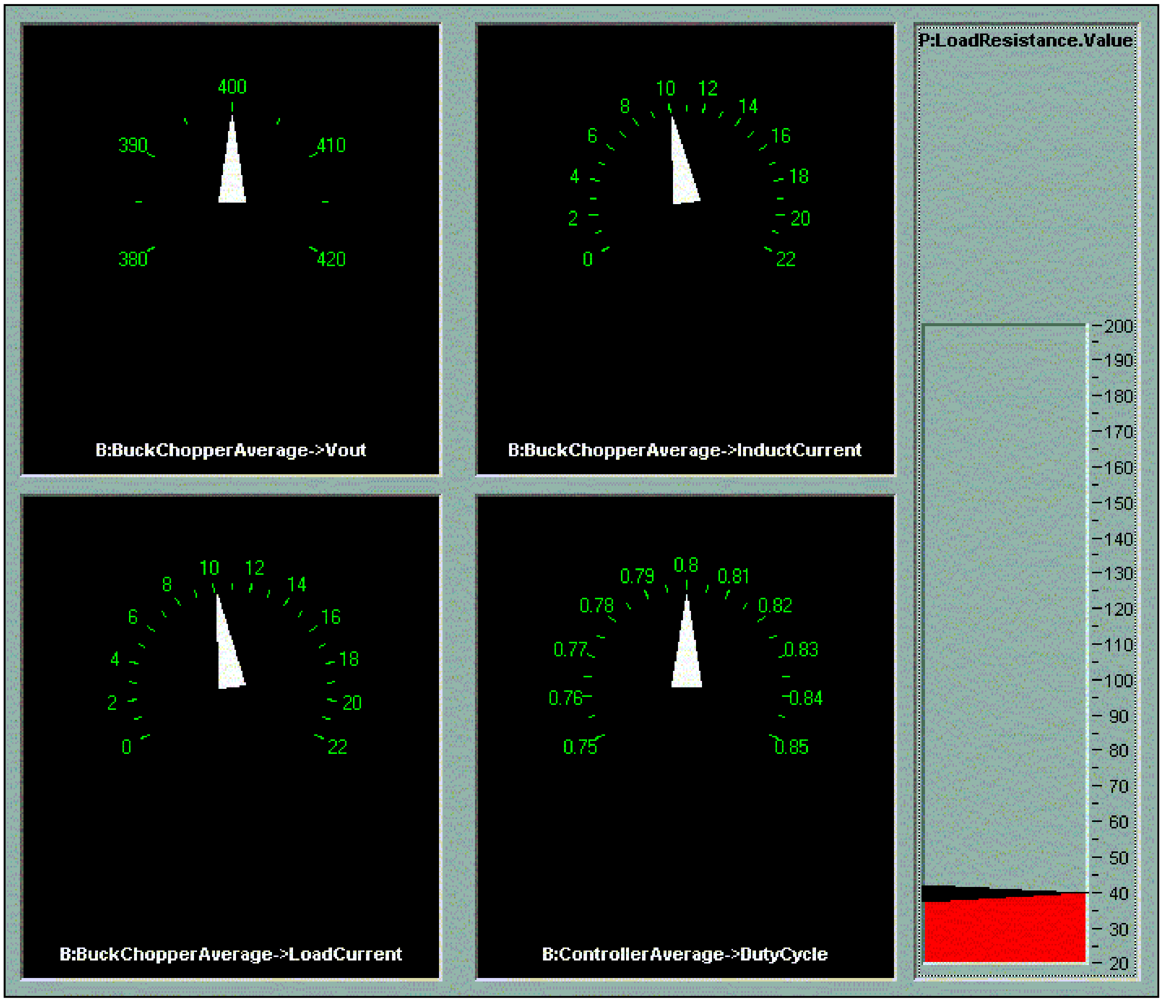

Figure E-35.

The dSPACE controller board is fully described in Reference [24]. When hooking up dSPACE to hardware, ensure the control signals are powered up first then power can be applied to the control circuitry.

In summary, dSPACE has facilitated the testing of a hardware controller prior to the completion of the buck chopper power section. A SIMULINK model was created for a buck chopper and then compiled to run in dSPACE. The dSPACE environment was then entered and a control desk created to enable the control of load resistance of our model. Once the dSPACE buck chopper was interfaced with the hardware controller, via the dSPACE i/o board, the stability of the controller was accessed. As the above results show, the controller is stable between 20 and 200 Ohms of load resistance. It outputs 400 Volts and has an 80% duty cycle.

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